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CoreFPGA (TM) 3 Board Schematics

Dual FPGA Rev 1.0

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DRG_NUM: MD00474 Revision: 01.01
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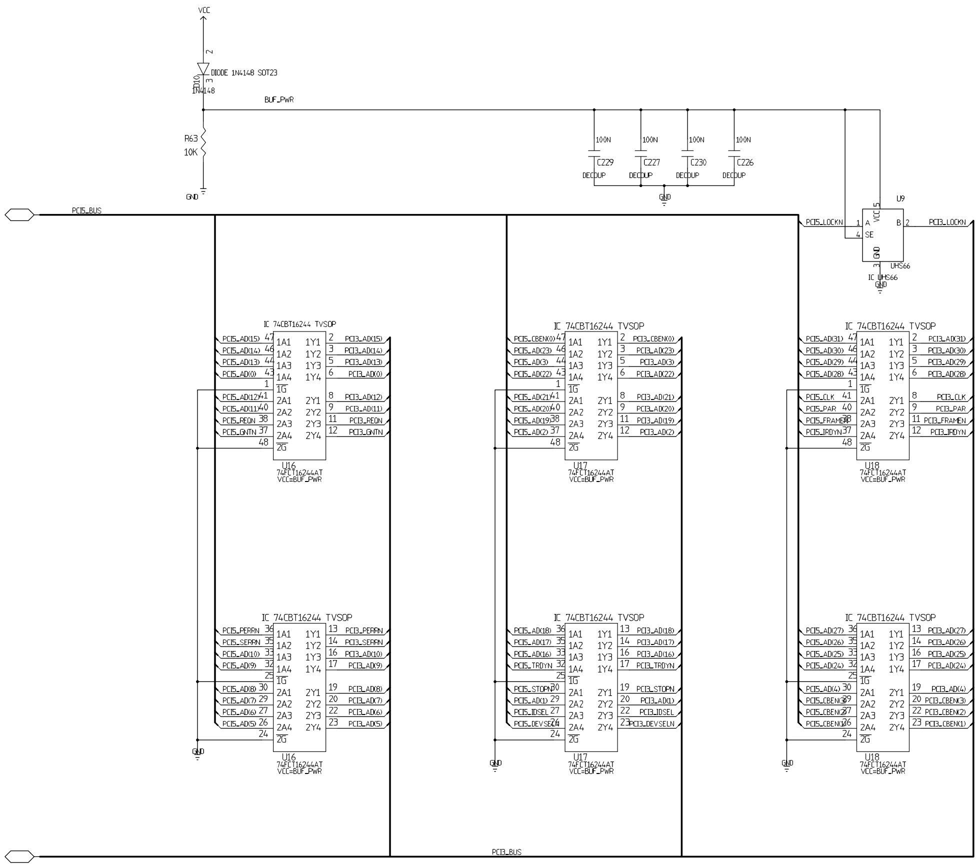

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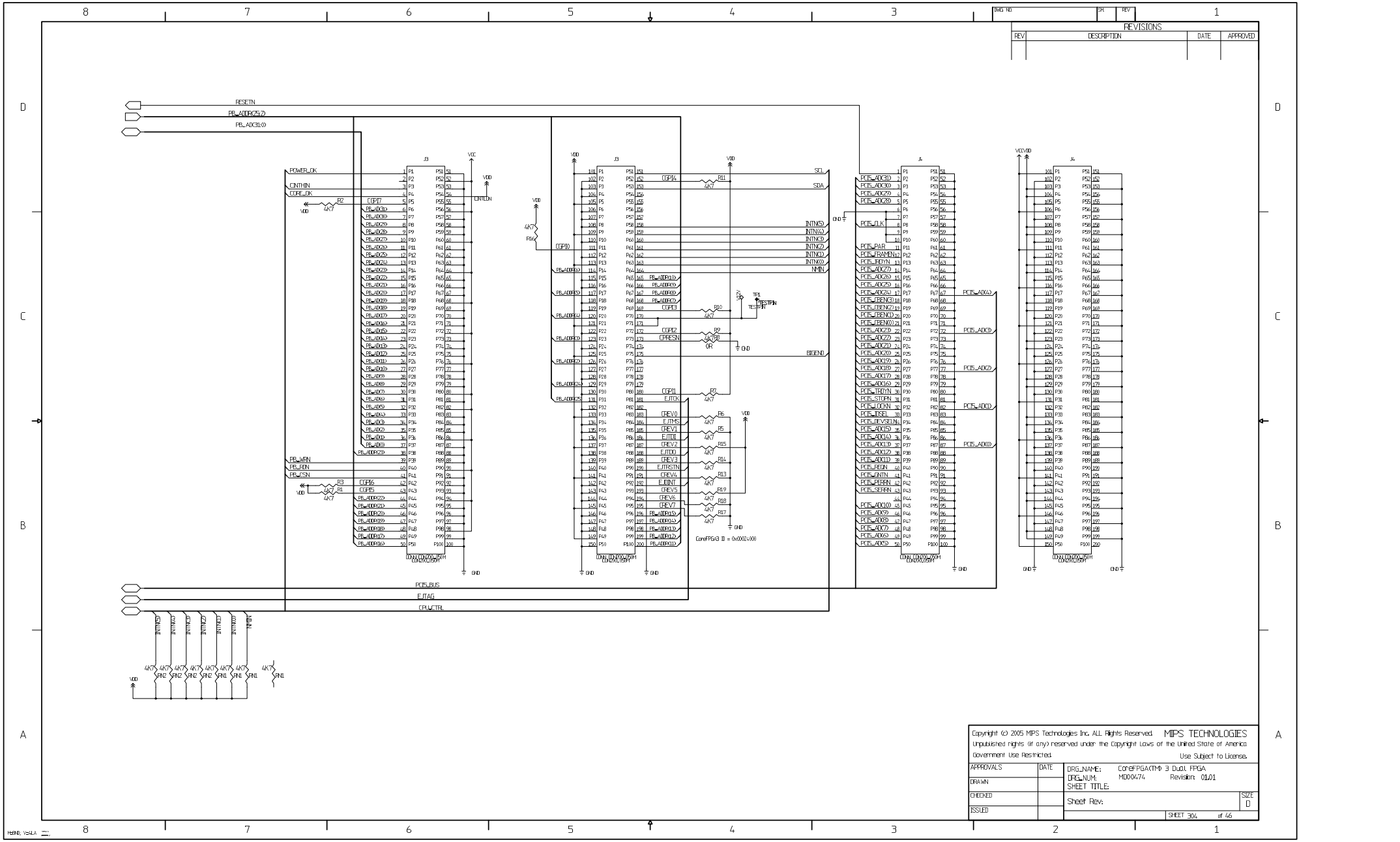

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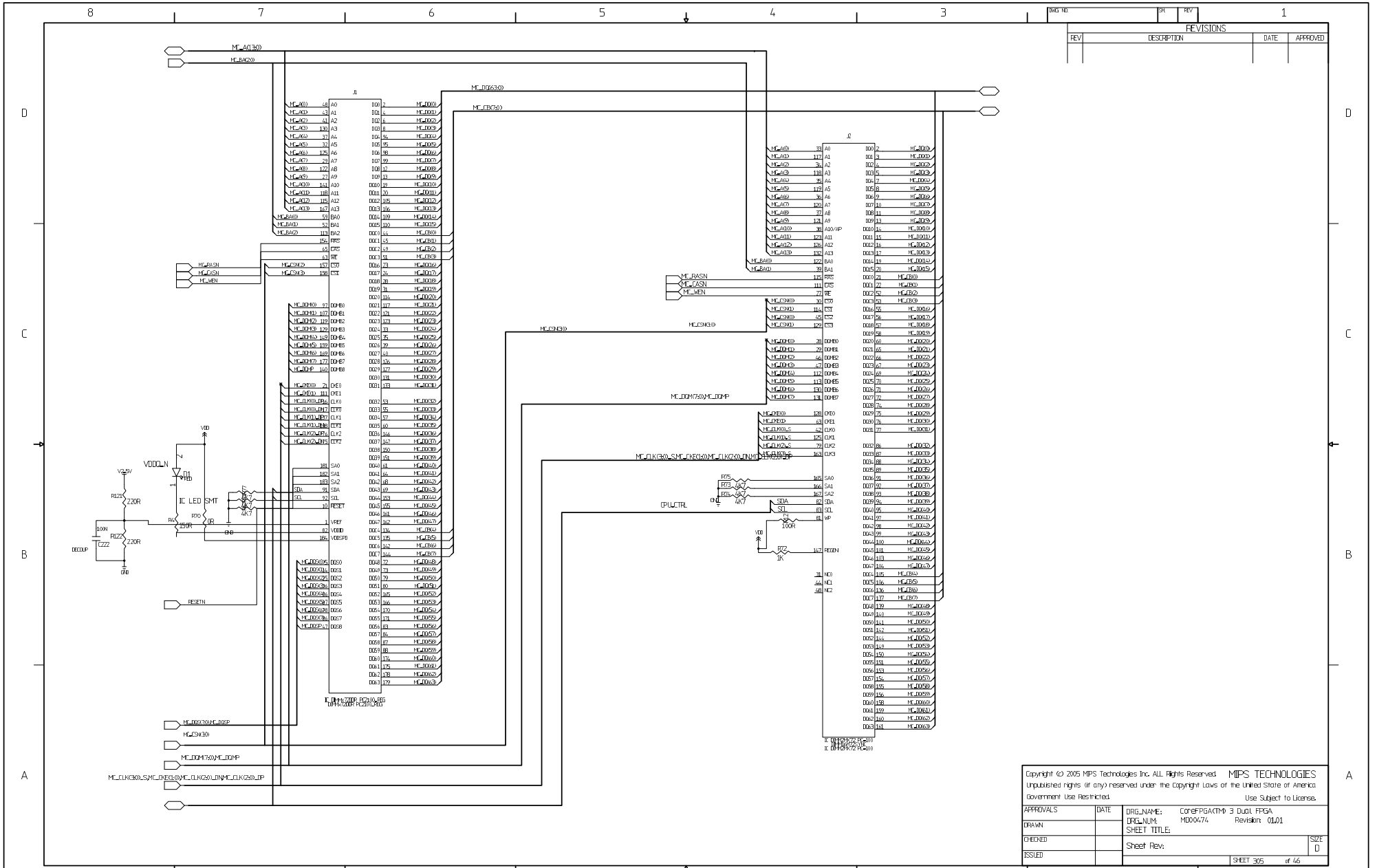

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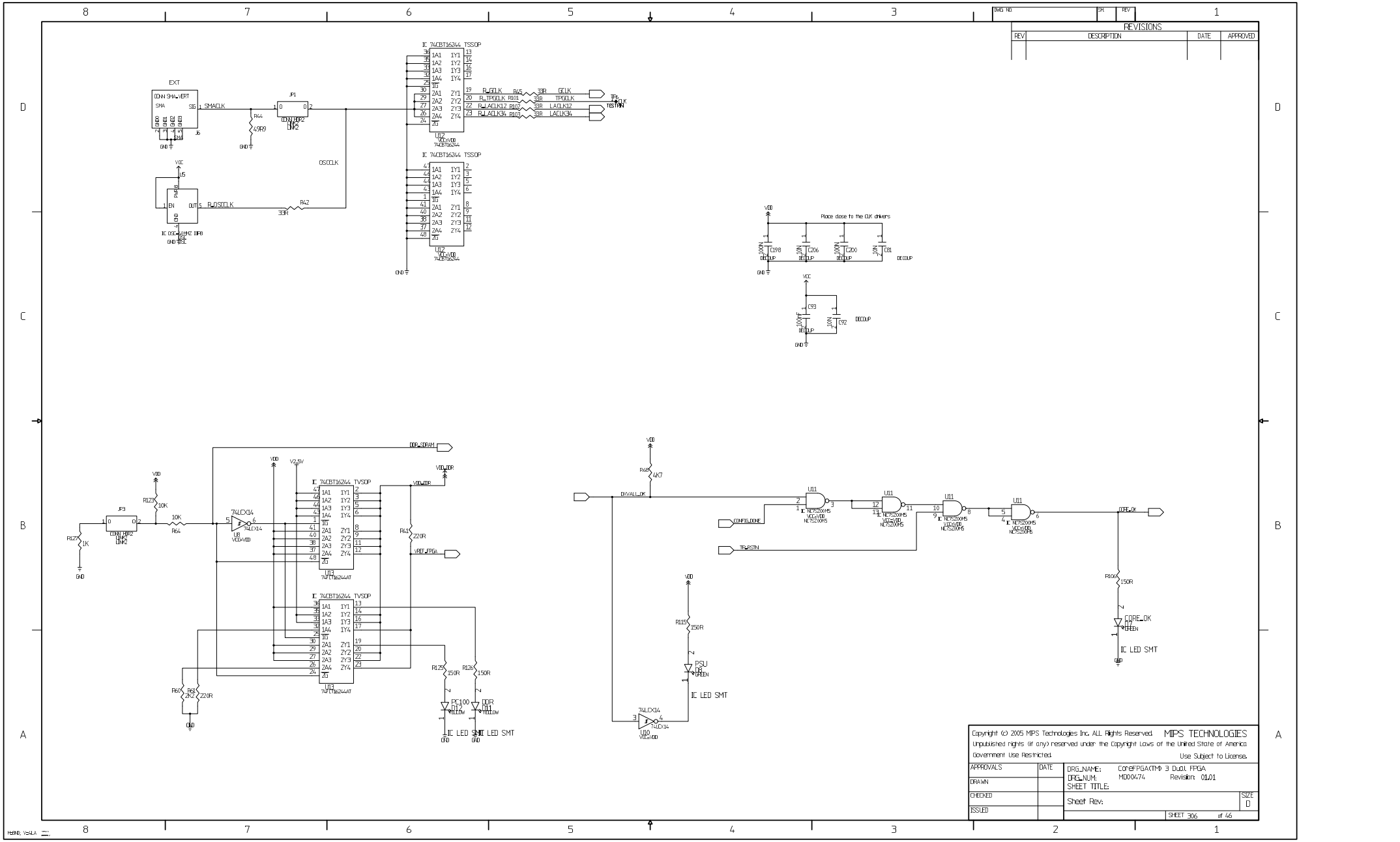

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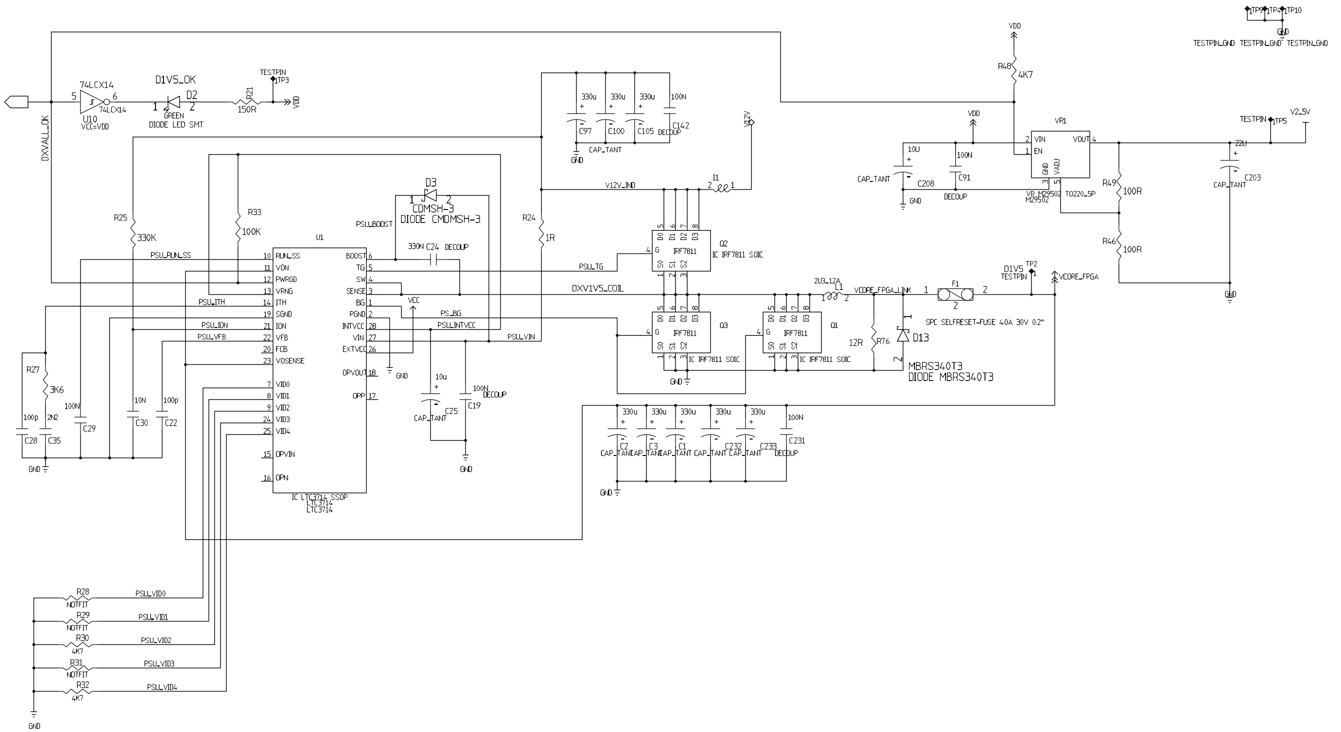

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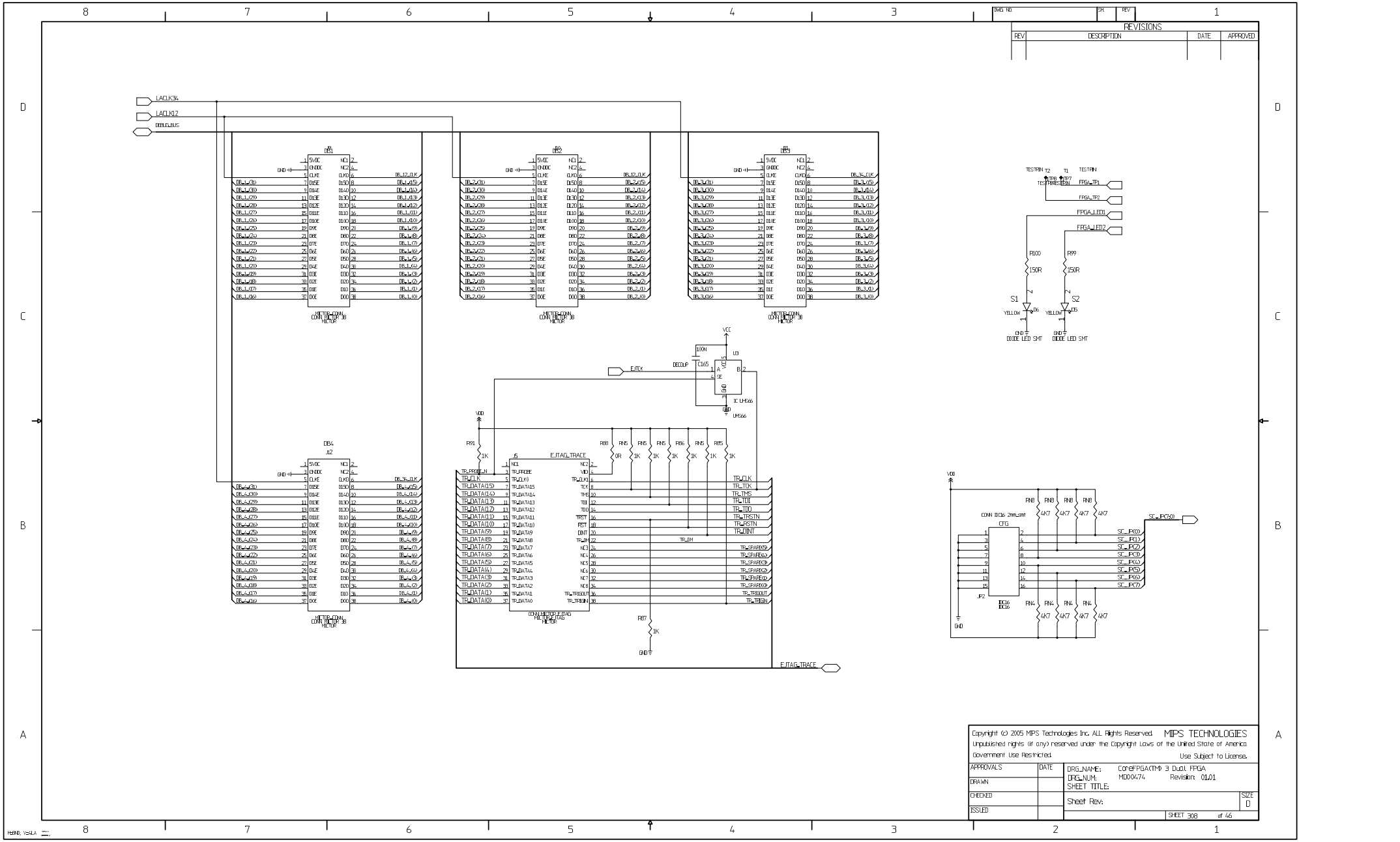

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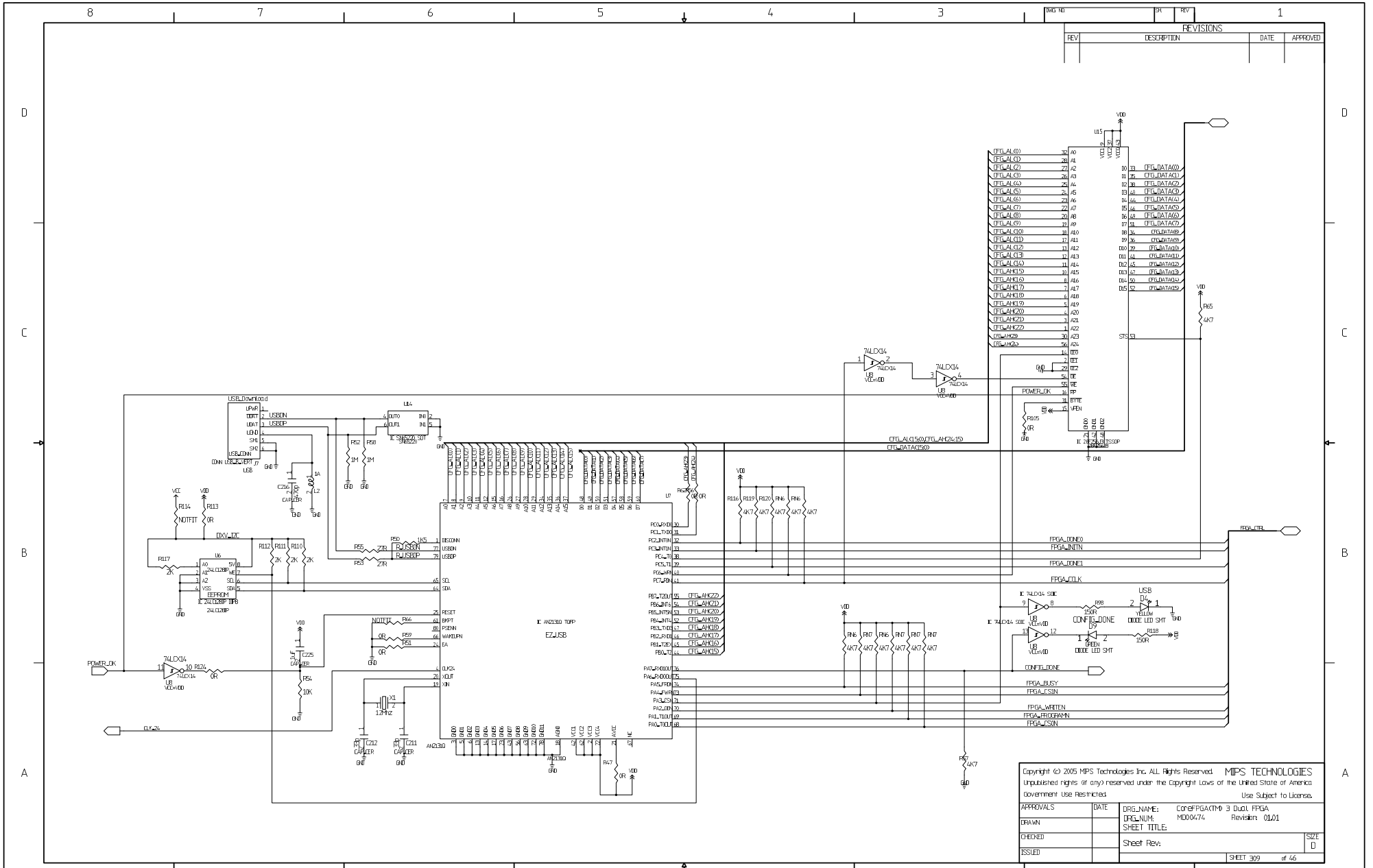

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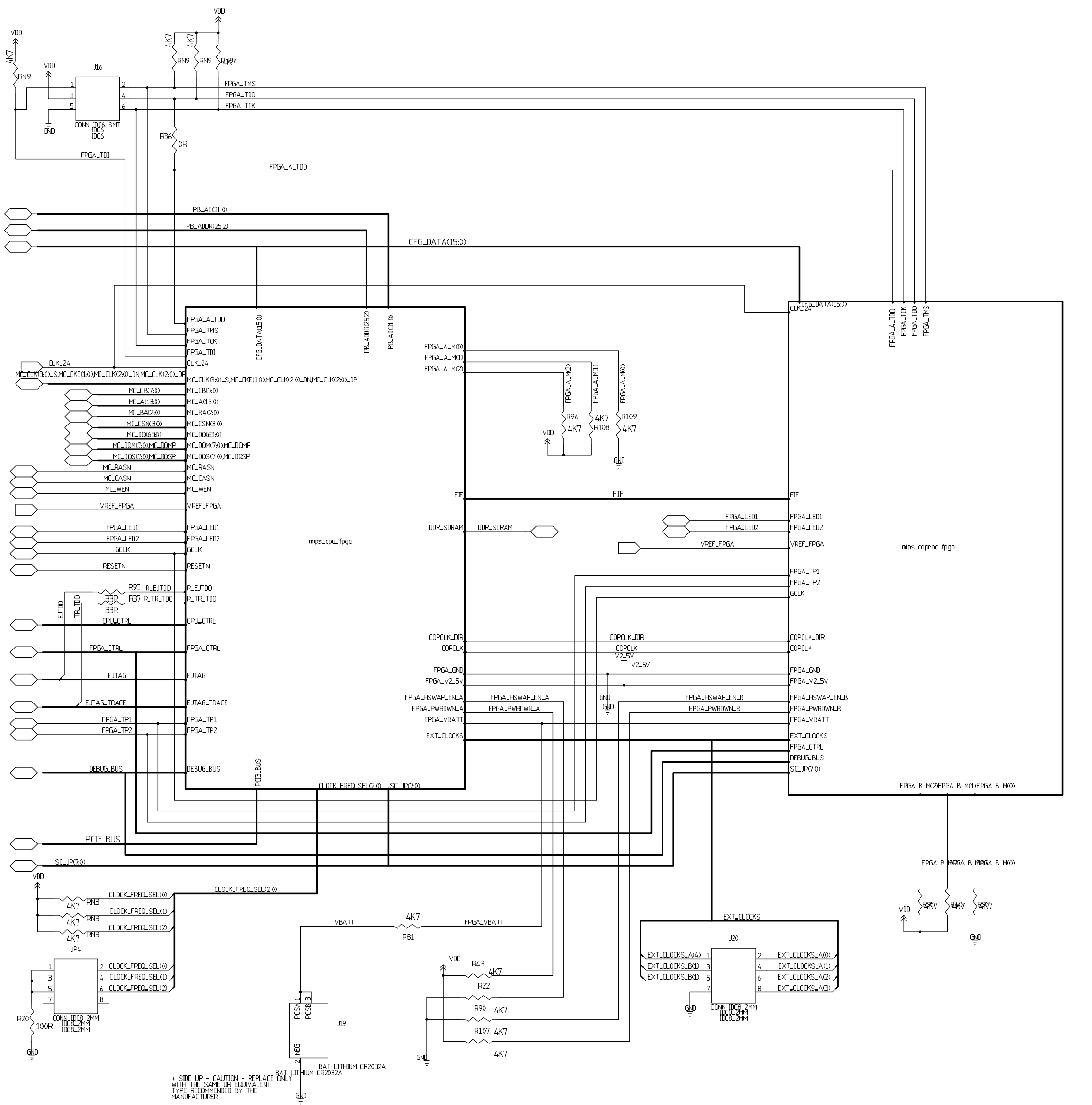

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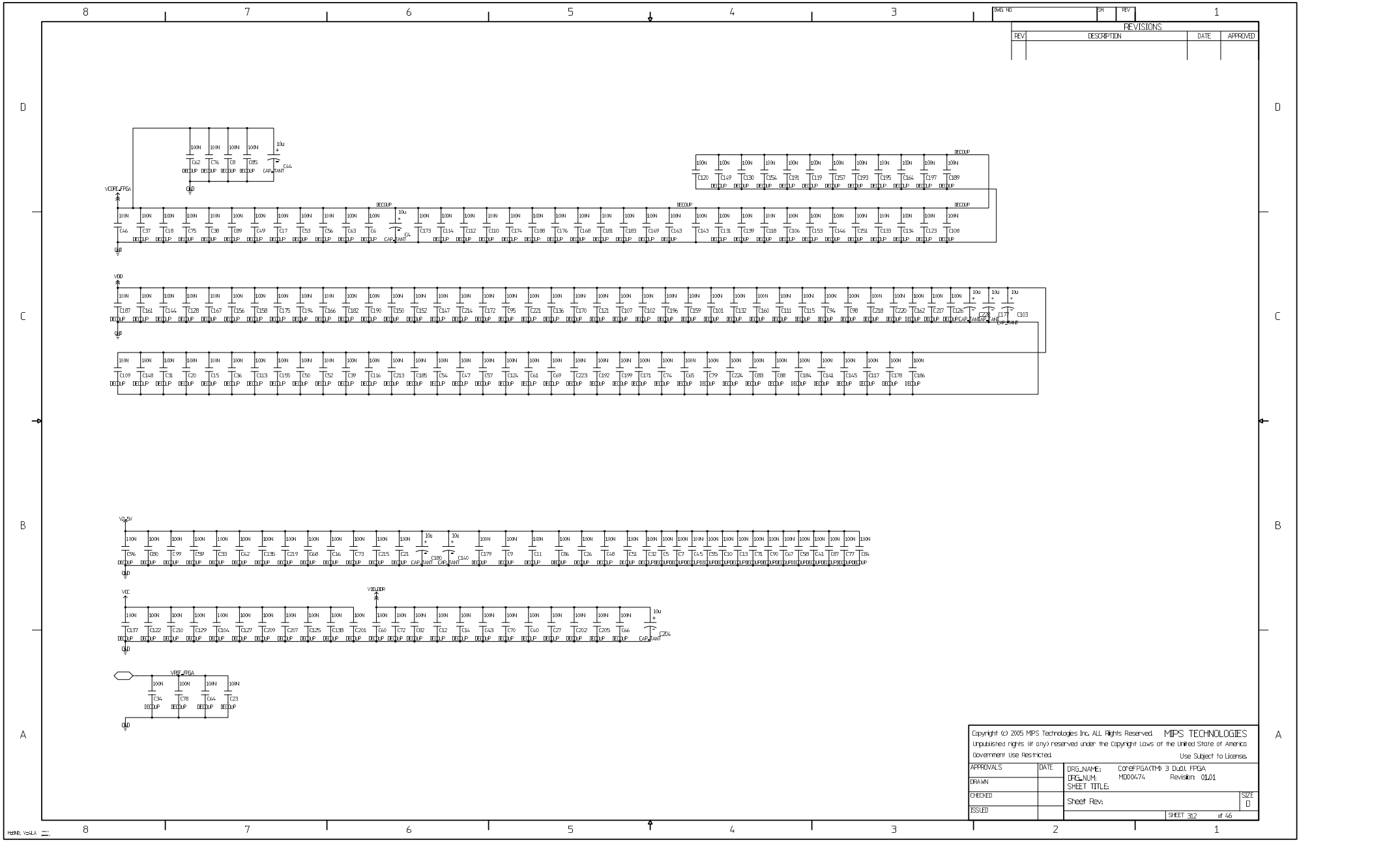

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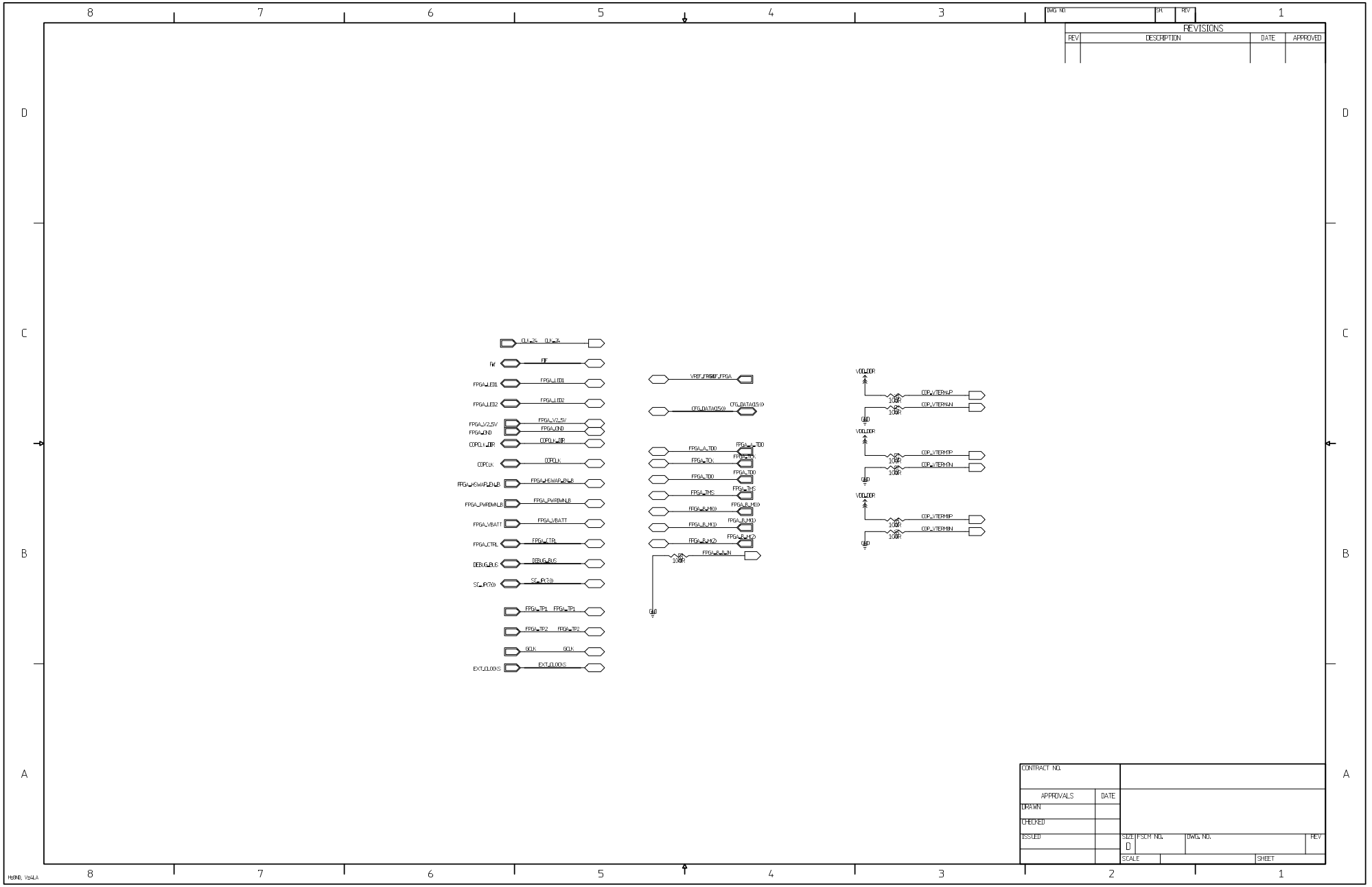

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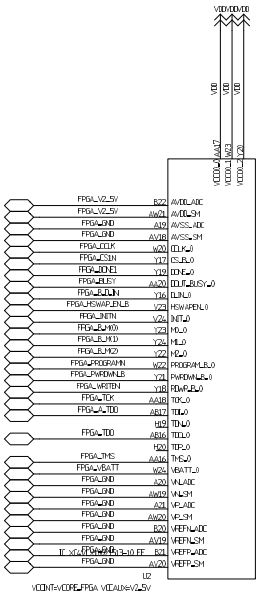

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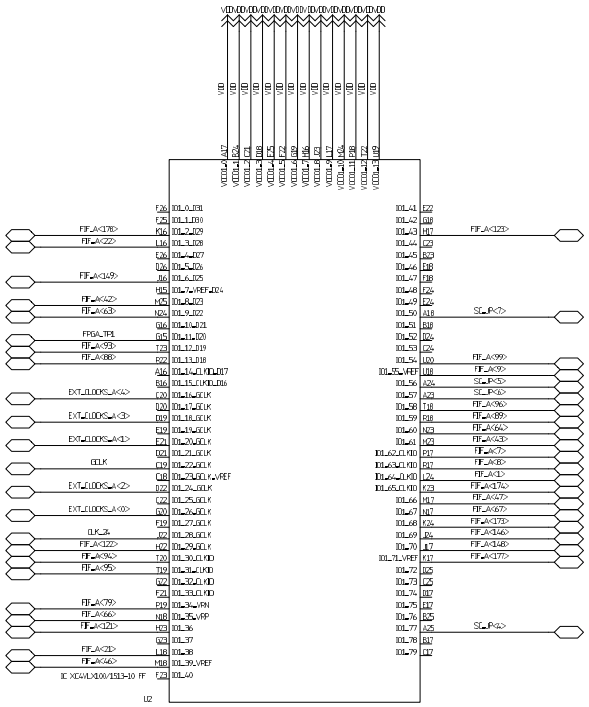

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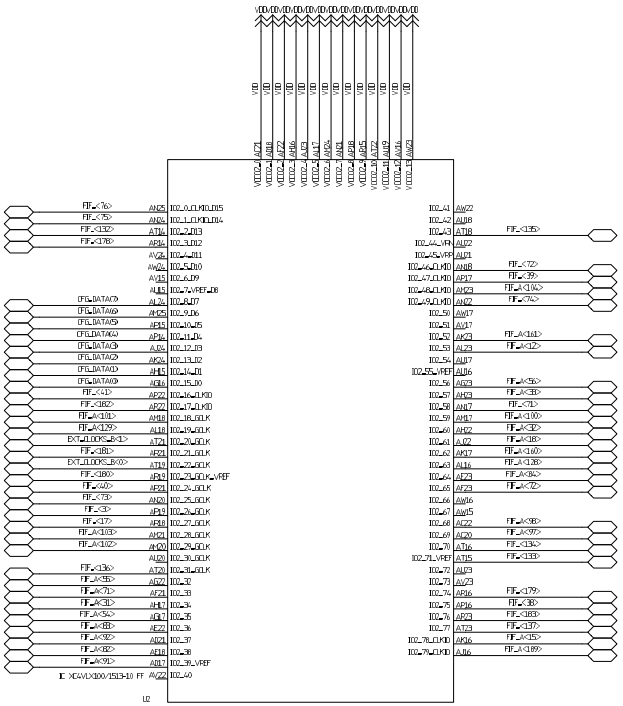

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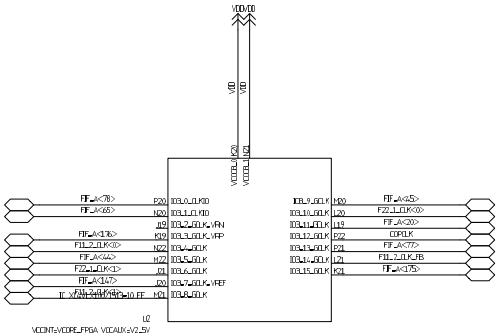

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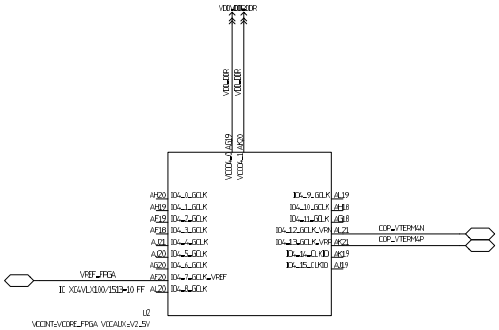

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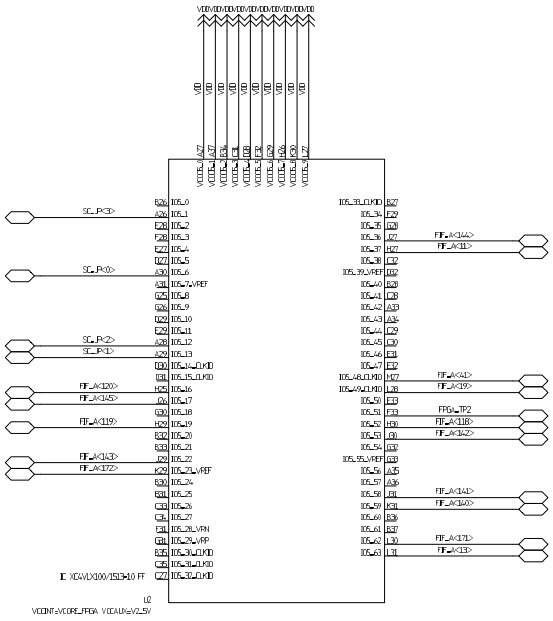

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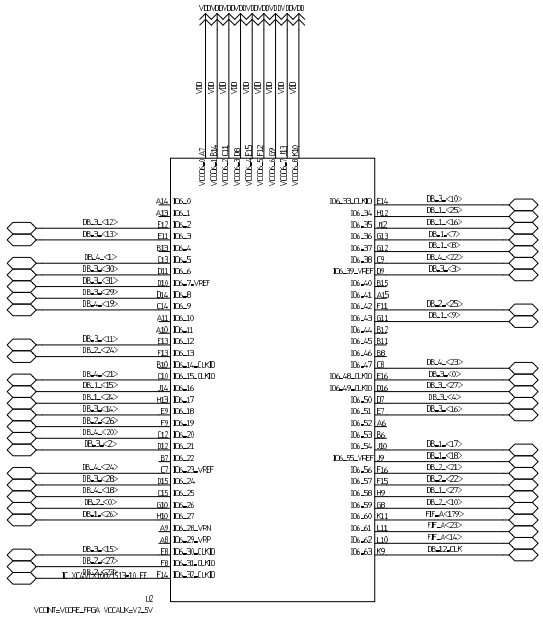

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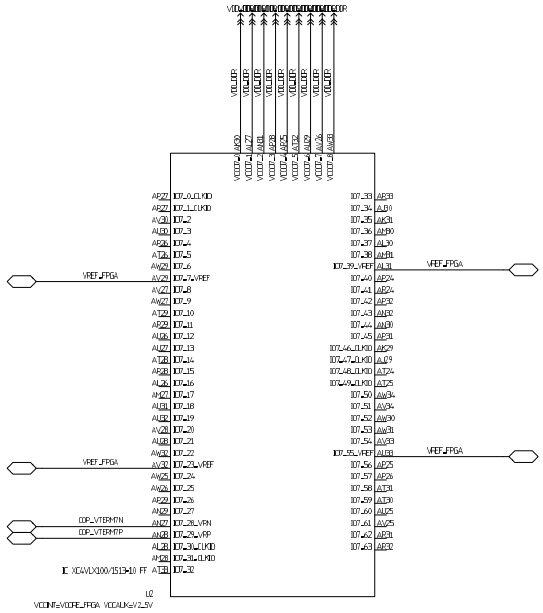

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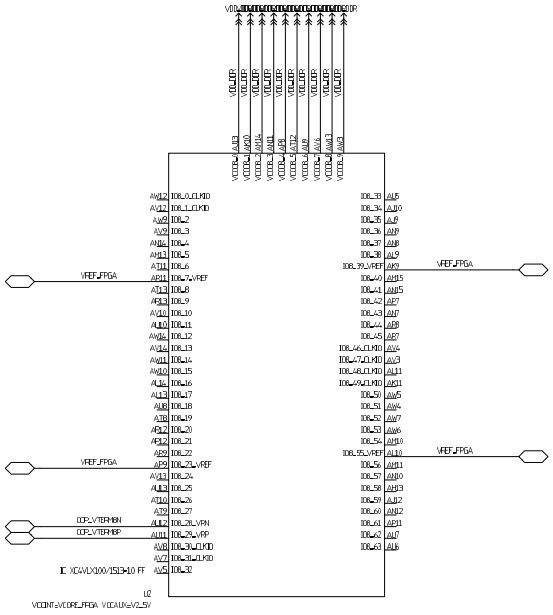

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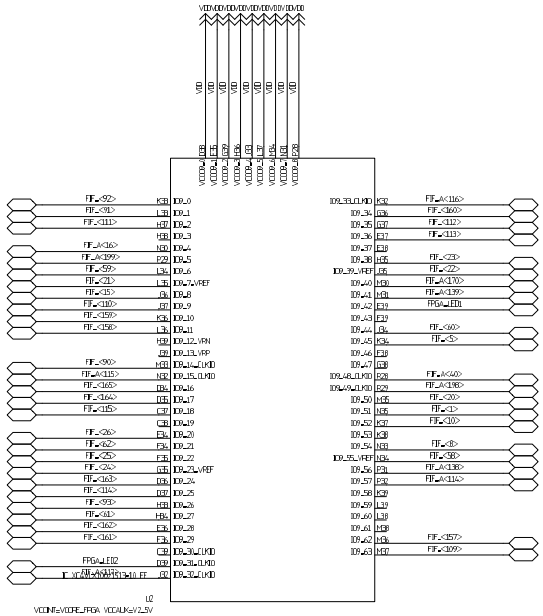

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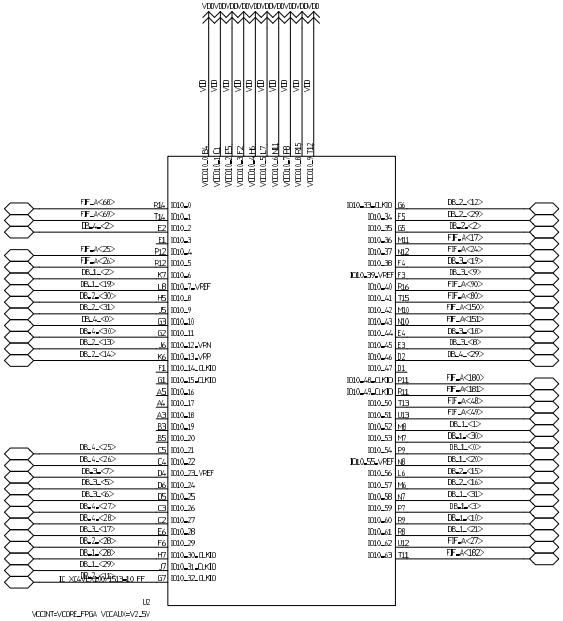

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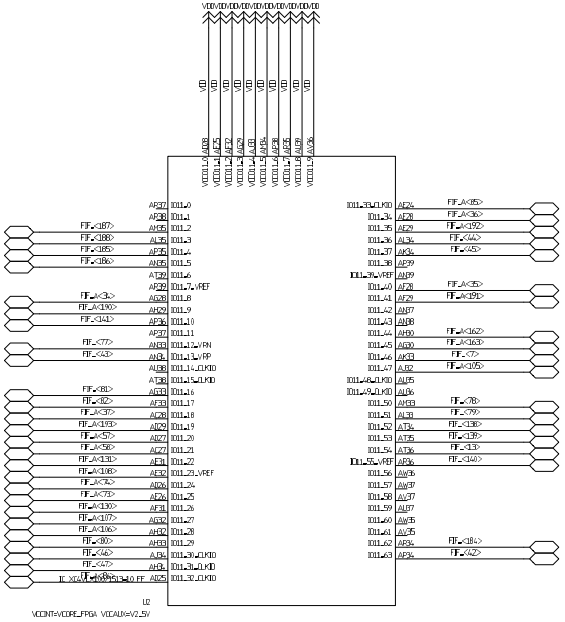

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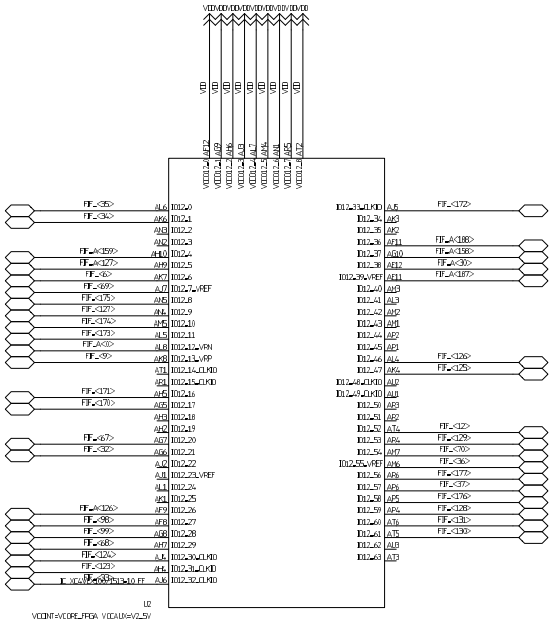

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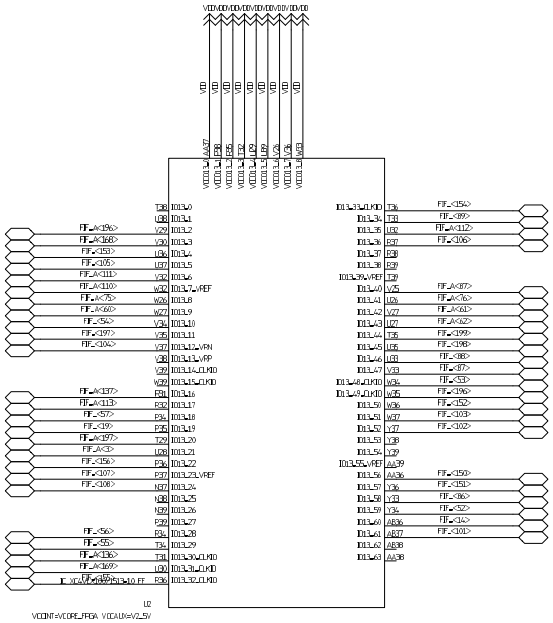

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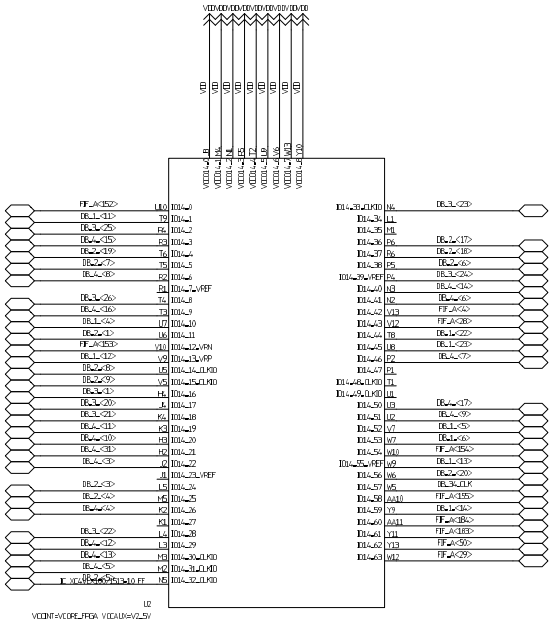

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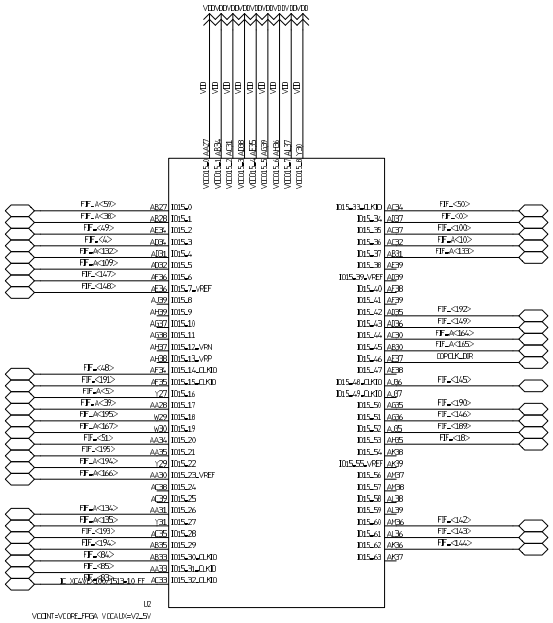

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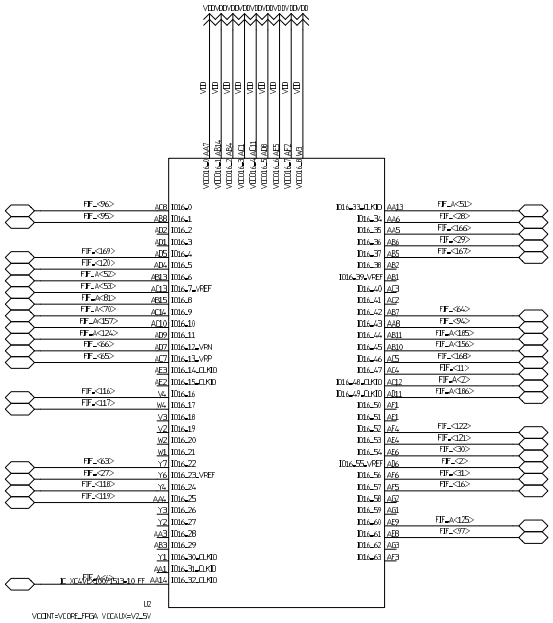

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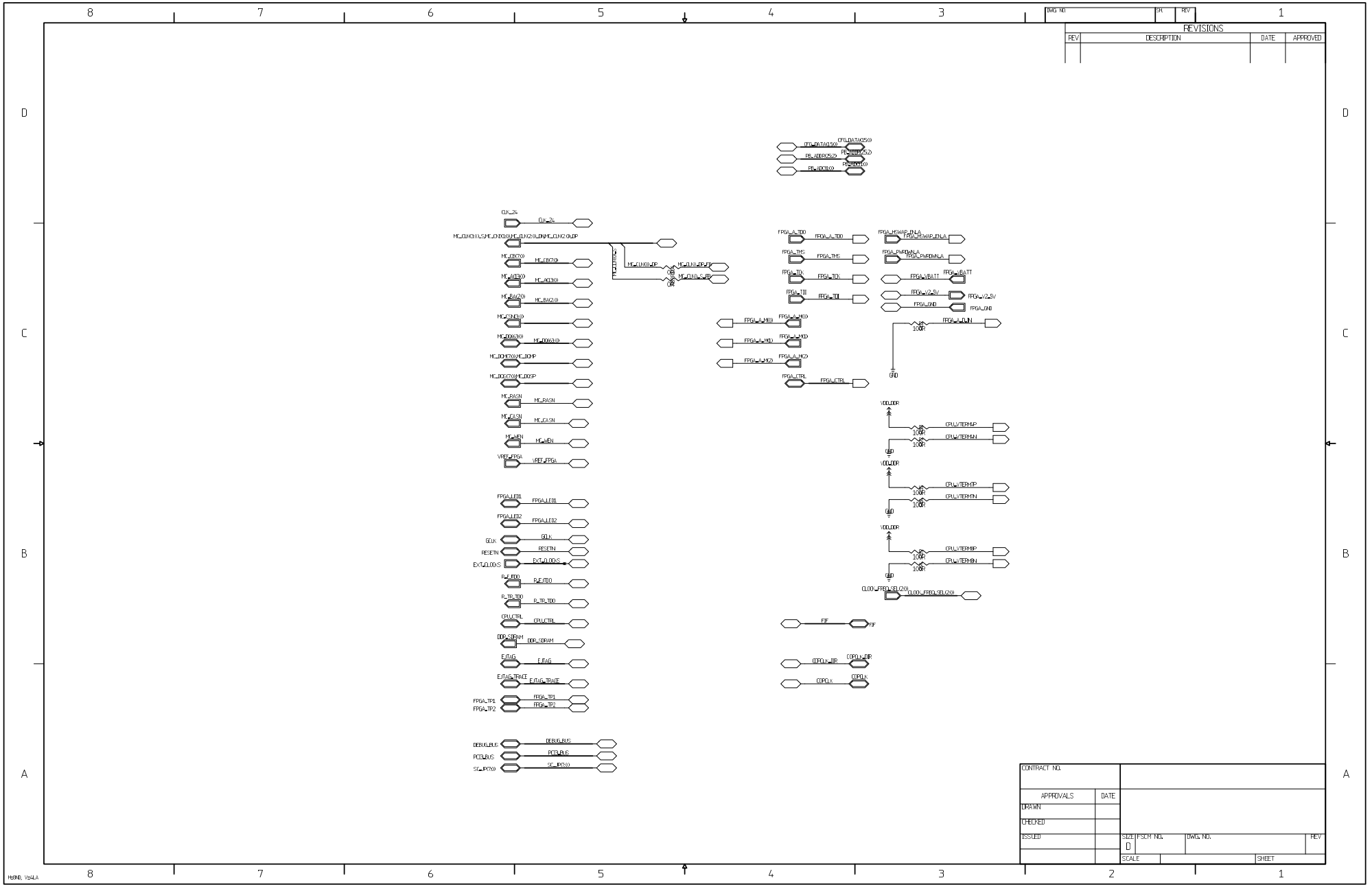
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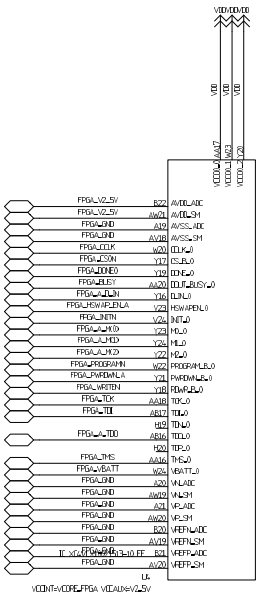

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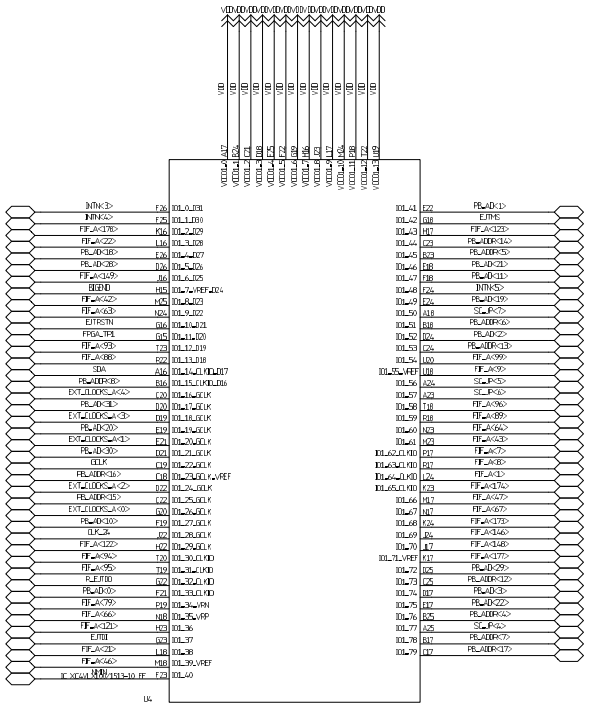

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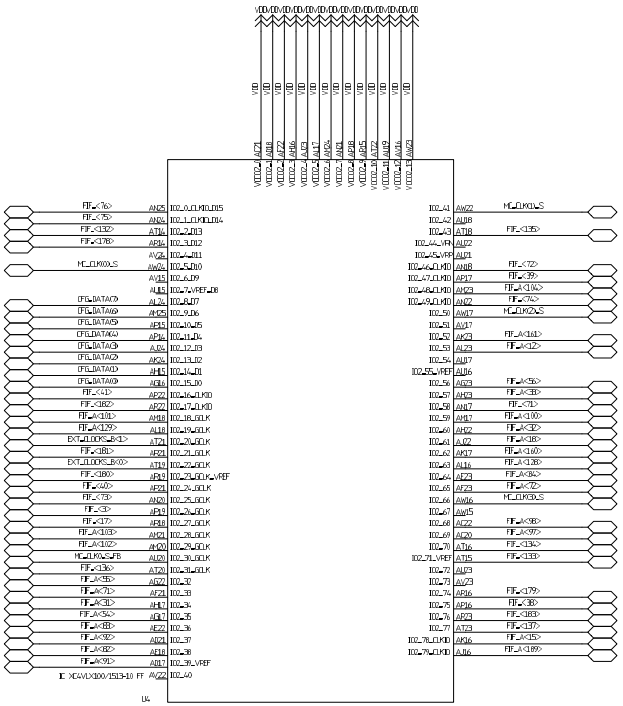

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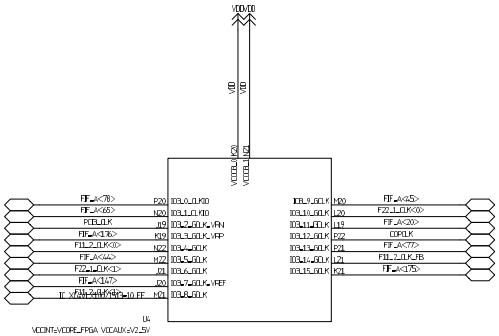

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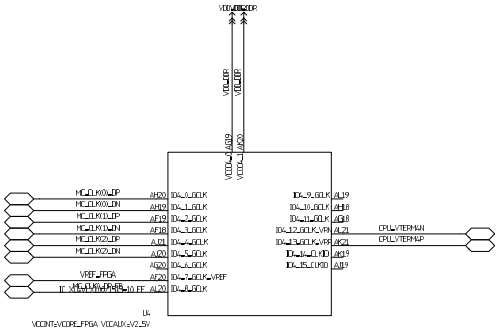

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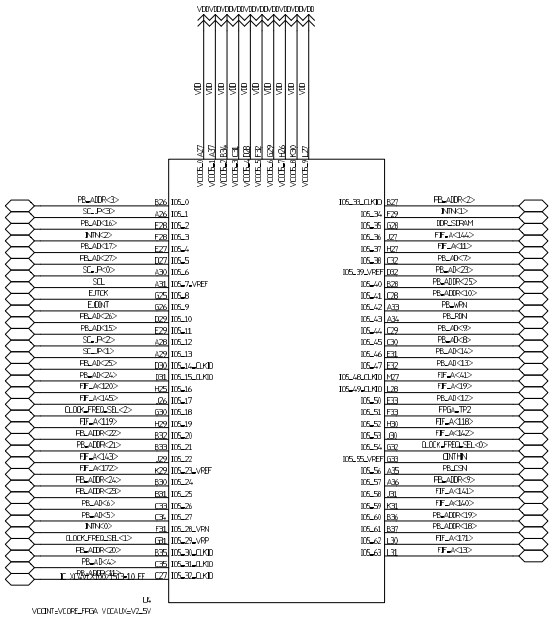

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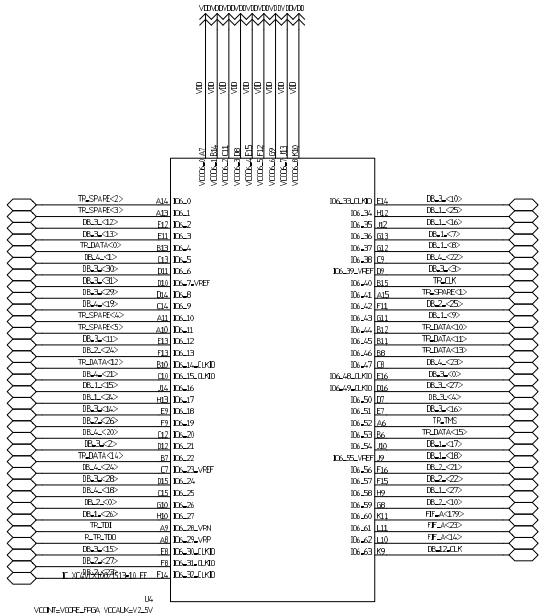

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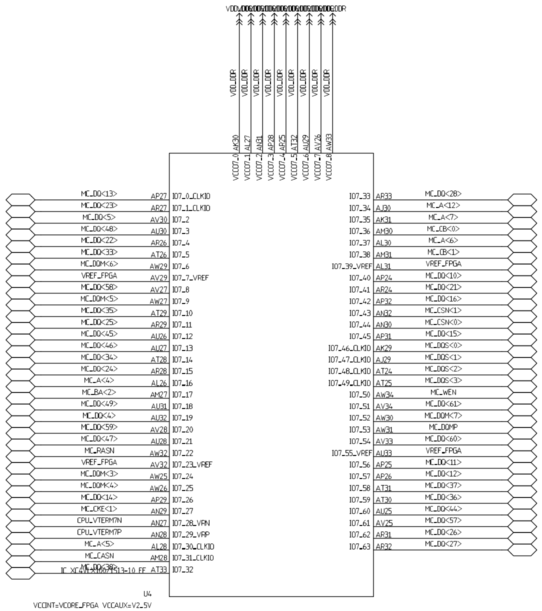

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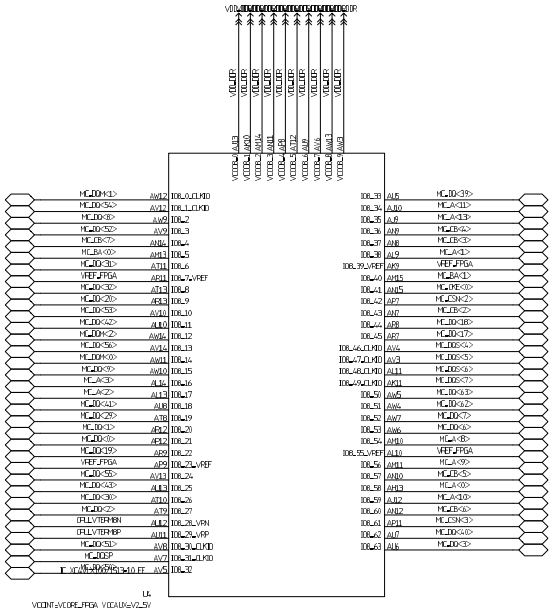

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SHEET 10 of 46

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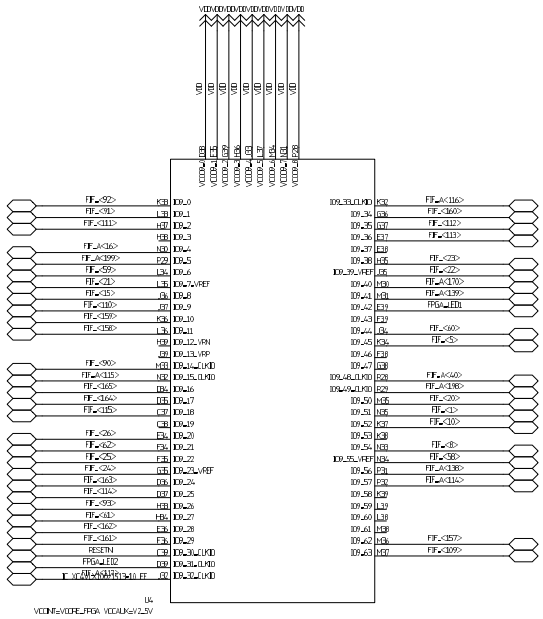

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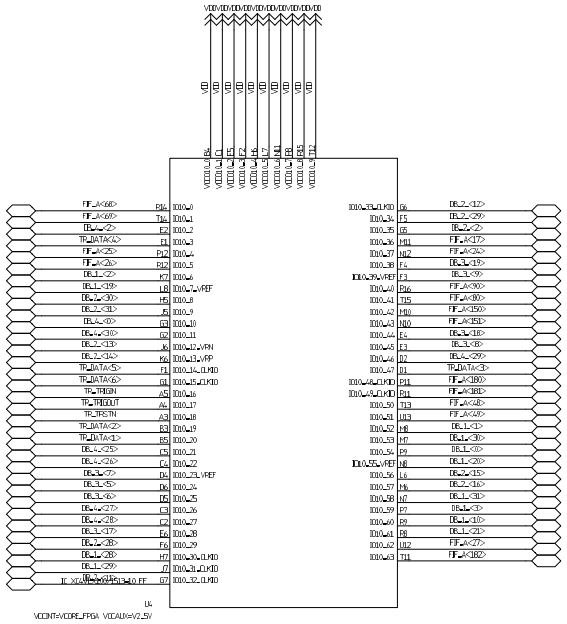

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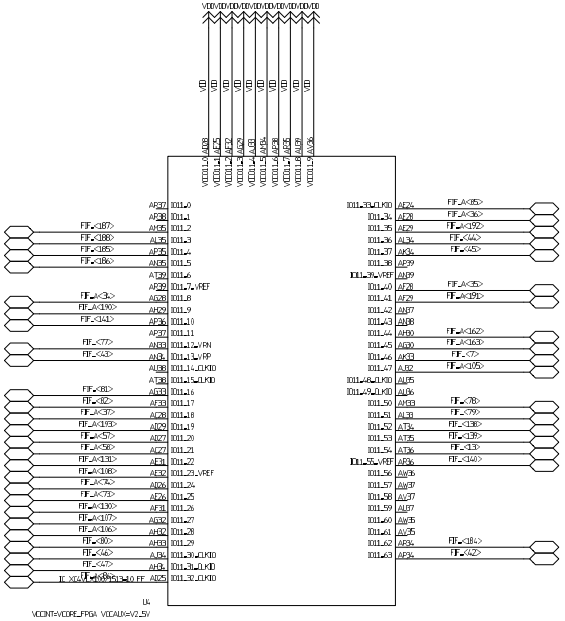

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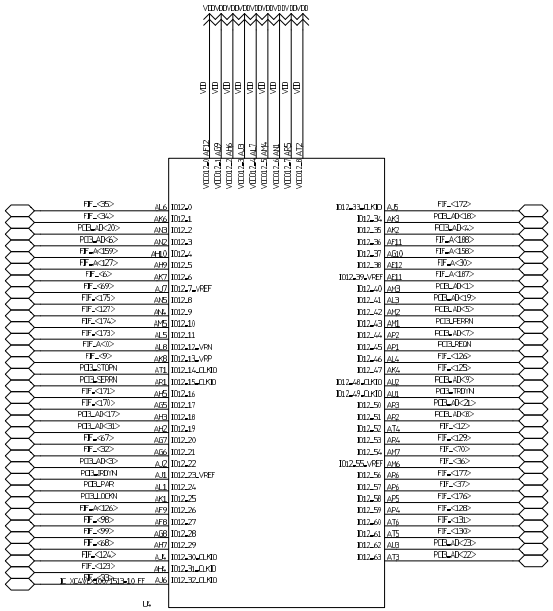

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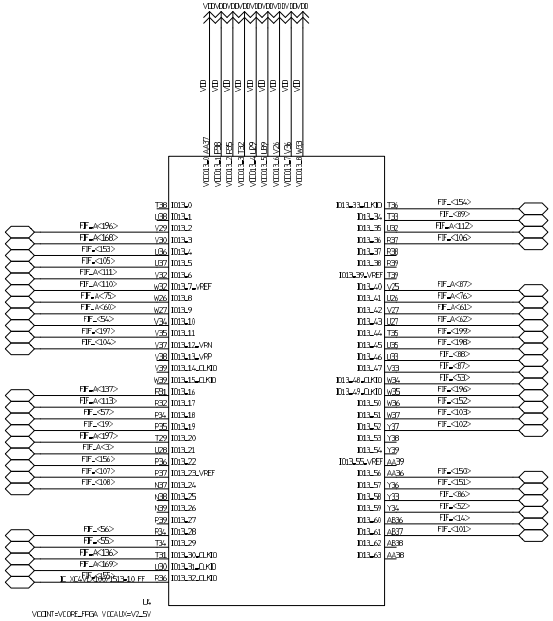

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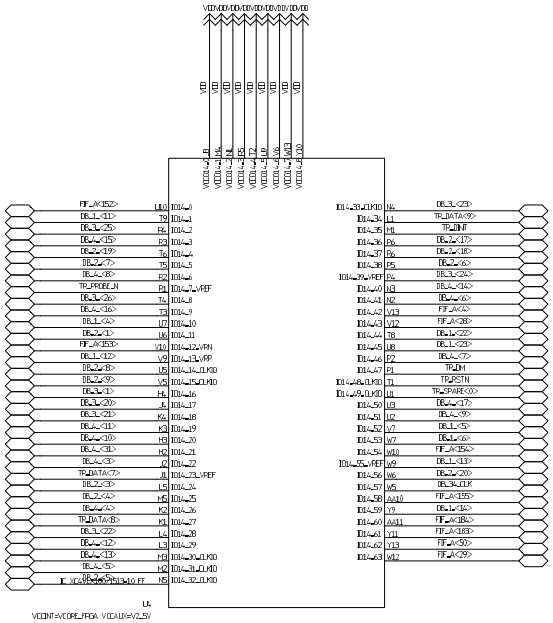
SHEET 15 of 46



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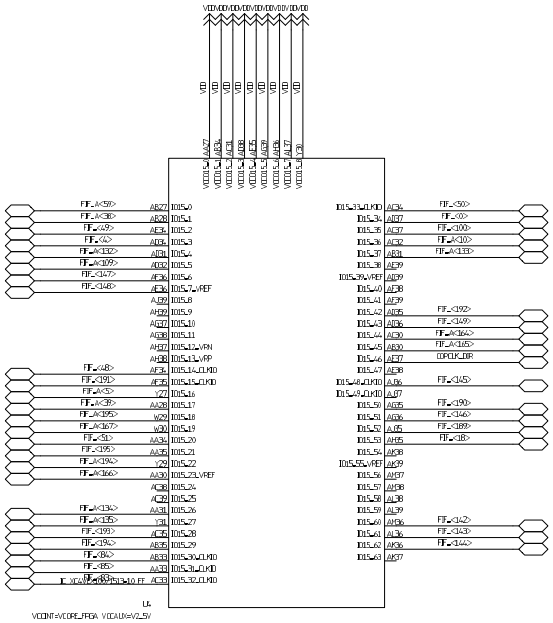

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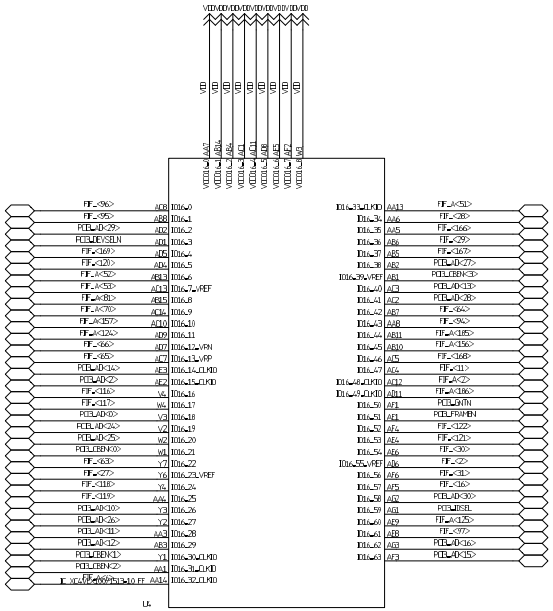

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SHEET 18 of 46