

CoreFPGA (TM) 3 Board Schematics

Dual FPGA Rev 1.0

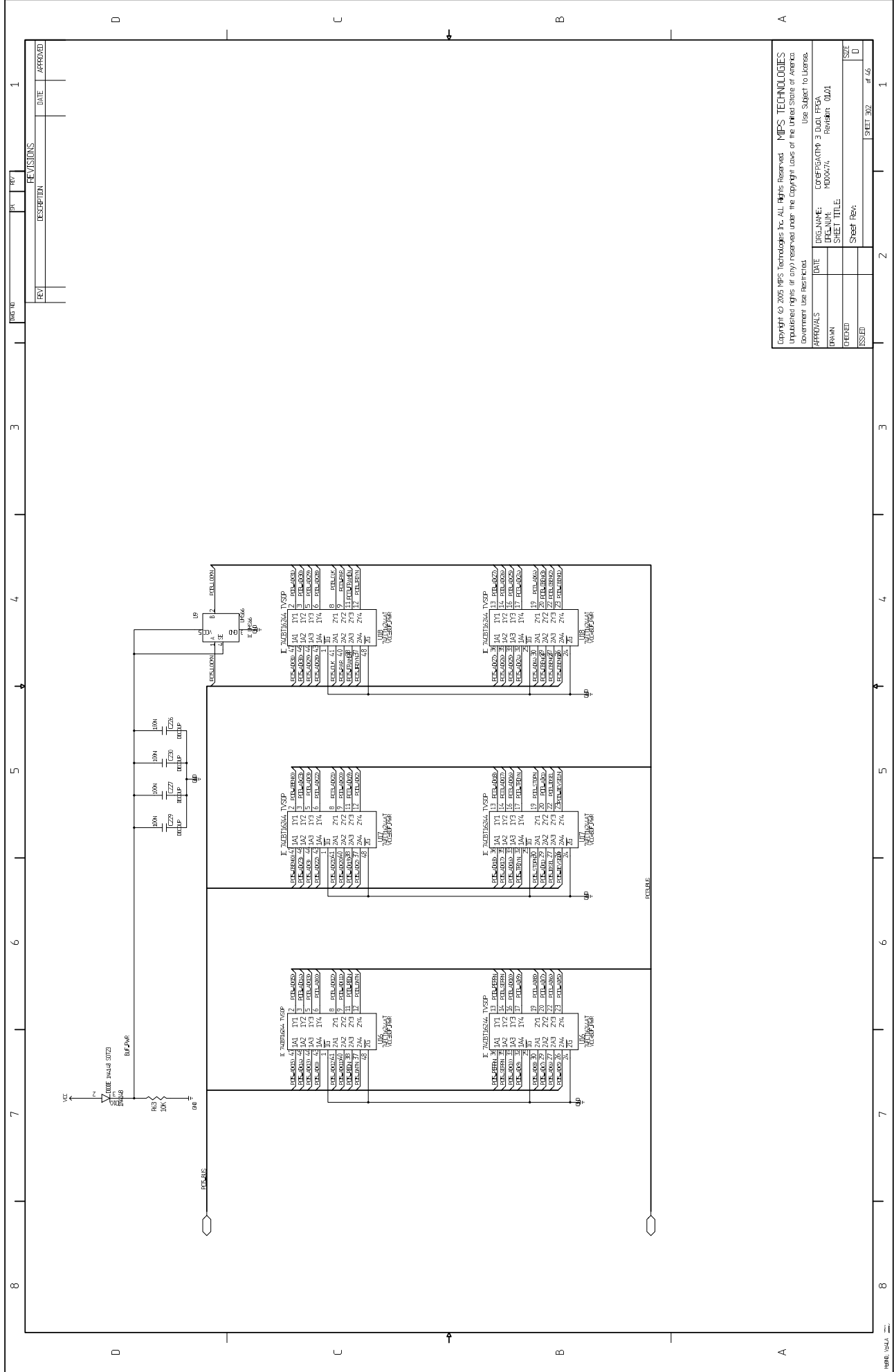
REV	DESCRIPTION	DATE	APPROVED

DATE	DESIGN NAME	DESIGN NUMBER	SHEET TITLE	SHEET REV.	SIZE

DATE	DRAWN	CHECKED	ISSUED

Copyright © 2005 MIPS Technologies, Inc. All Rights Reserved. MIPS TECHNOLOGIES
 Unpublished rights (if any) reserved under the Copyright Laws of the United States of America.
 Government Use Restricted. Use Subject to License.

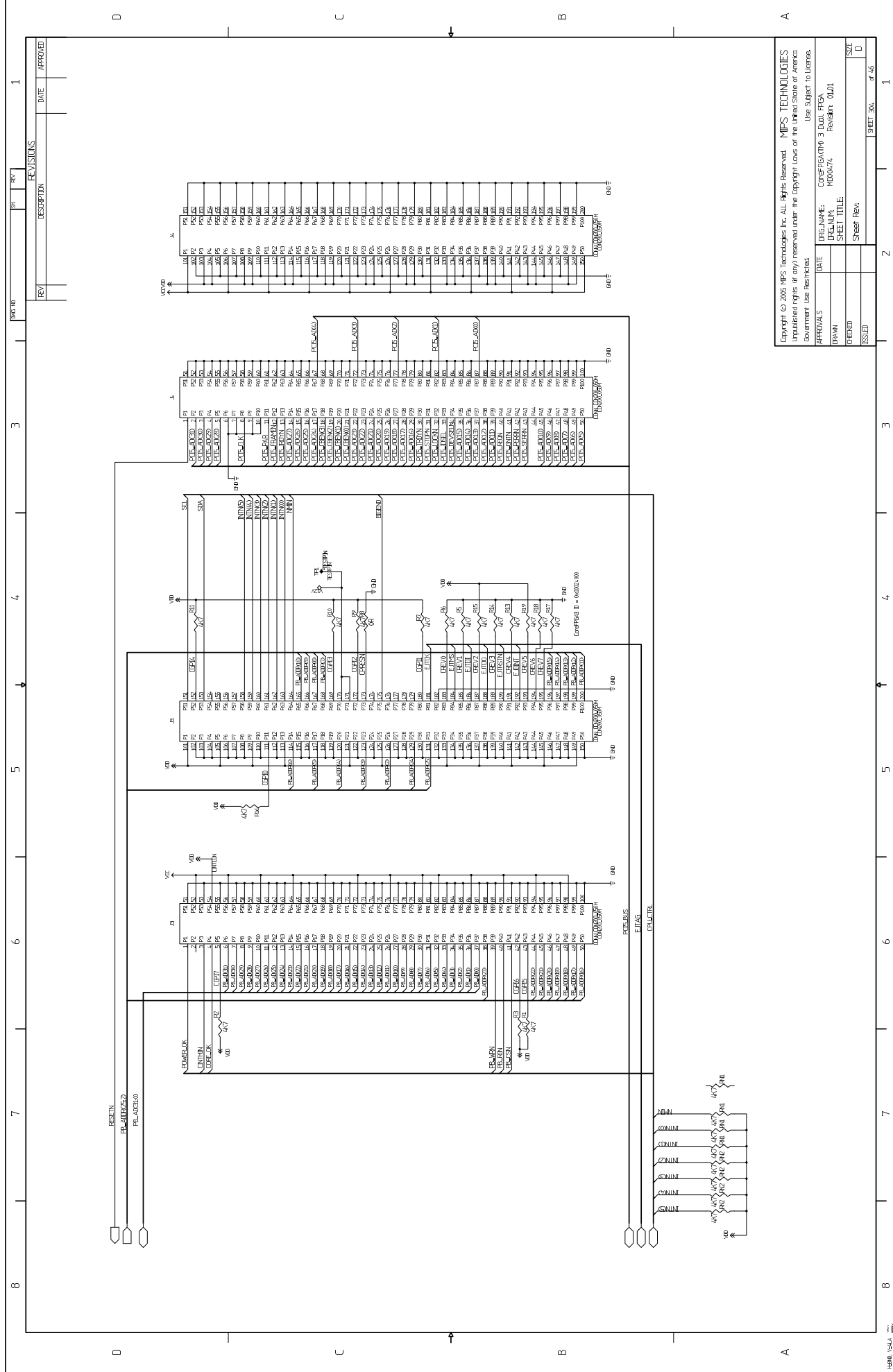
SHEET 301 of 46



REV	DESCRIPTION	DATE	APPROVED

APPROVALS		DATE	DESIGN NAME	PROJECT NO.	REVISION	SIZE
DRAWN	CHECKED	ISSUED	CONFIRMING 3 DUAL FPGA	H000074	0001	D
SHEET TITLE			SHEET REV.			
SHEET 302			OF 46			

Copyright © 2005 MIPS Technologies, Inc. All Rights Reserved. MIPS TECHNOLOGIES
 Unpublished rights (if any) reserved under the Copyright Laws of the United States of America.
 Government Use Restricted. Use Subject to License.



REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

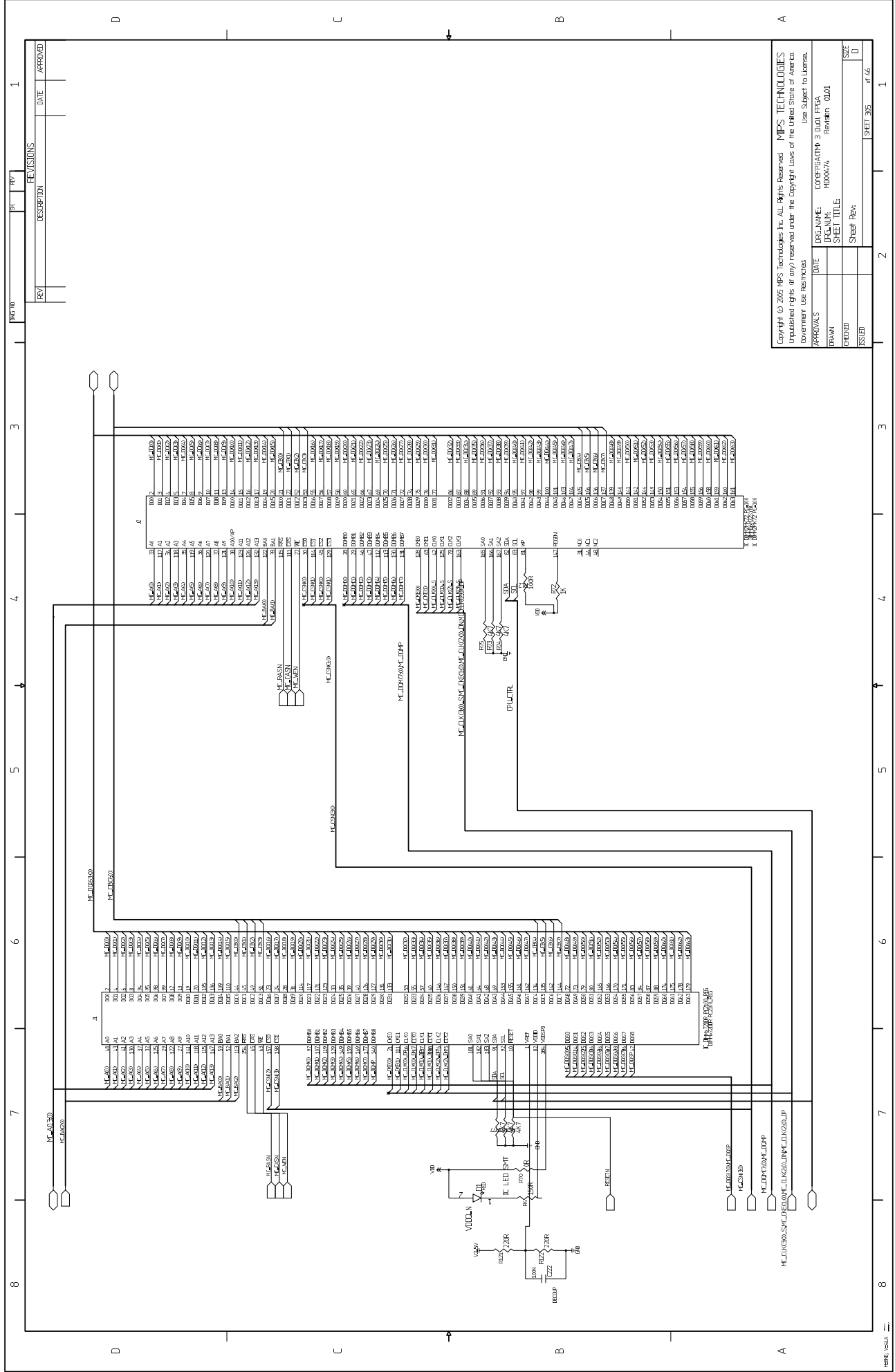
REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

Copyright © 2005 MIPS Technologies, Inc. All Rights Reserved. MIPS TECHNOLOGIES Unpublished rights reserved under the Copyright Laws of the United States of America. Government Use Restricted.			
DATE	DESIGNER	DATE	DESIGNER
CHECKED	DESIGN NAME	CHECKED	DESIGN NAME
ISSUED	SHEET NUMBER	ISSUED	SHEET NUMBER
	Sheet Rev:		Sheet Rev:



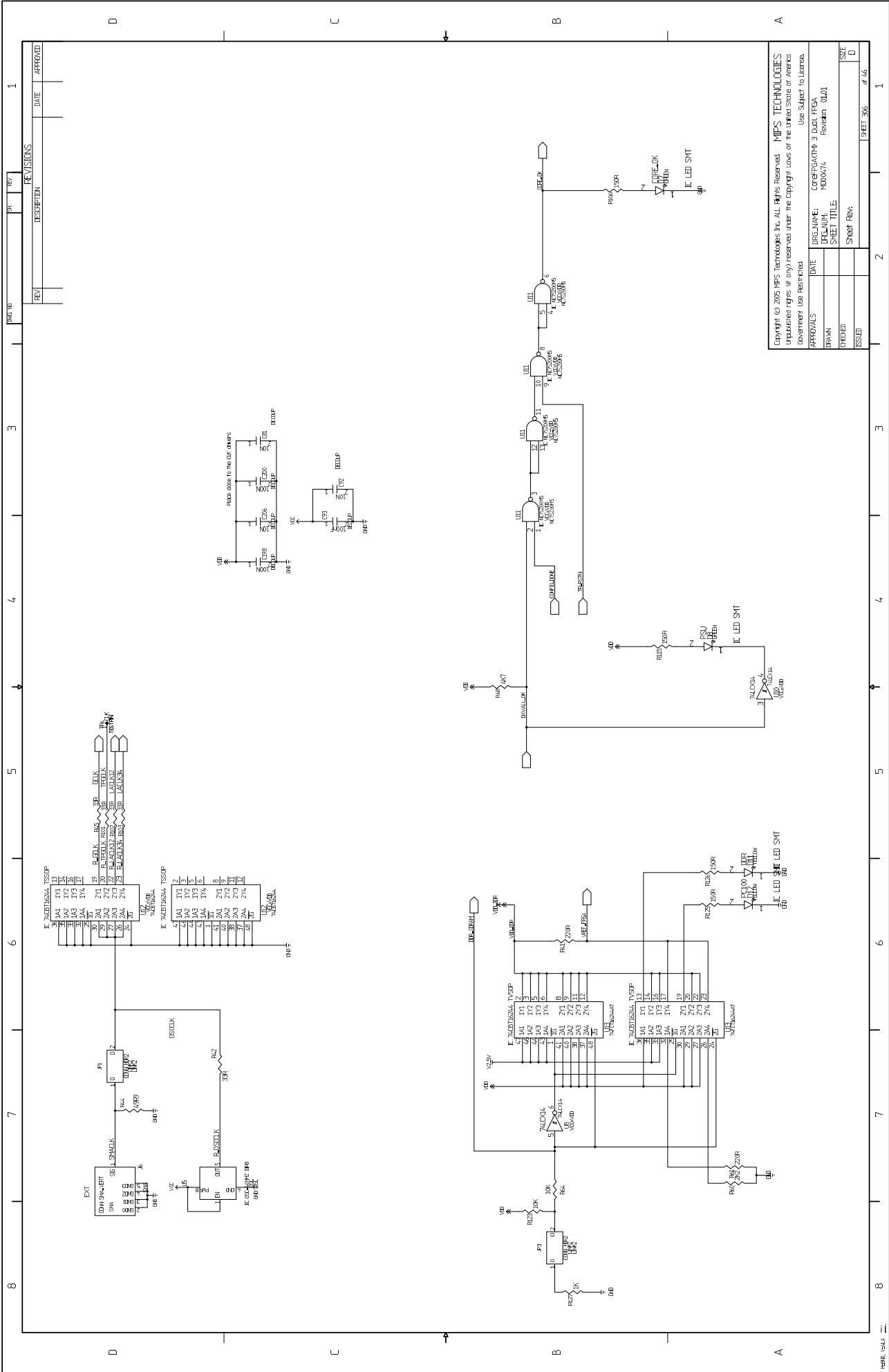
REV	REV	DESCRIPTION	DATE	APPROVED

Copyright © 2005 MIPS Technologies, Inc. All Rights Reserved. MIPS TECHNOLOGIES
 Unpublished rights reserved under the Copyright Laws of the United States of America
 Government Use Restricted

DATE: 09/29/05
 DES. NAME: COREFACTORY 3 Dual FPGA
 DDL NBR: 10000474
 SHEET TITLE: Sheet Title
 SHEET REV: 0.01

APPROVALS
 DRAWN:
 CHECKED:
 ISSUED:

SIZE: D
 SHEET 305 of 46

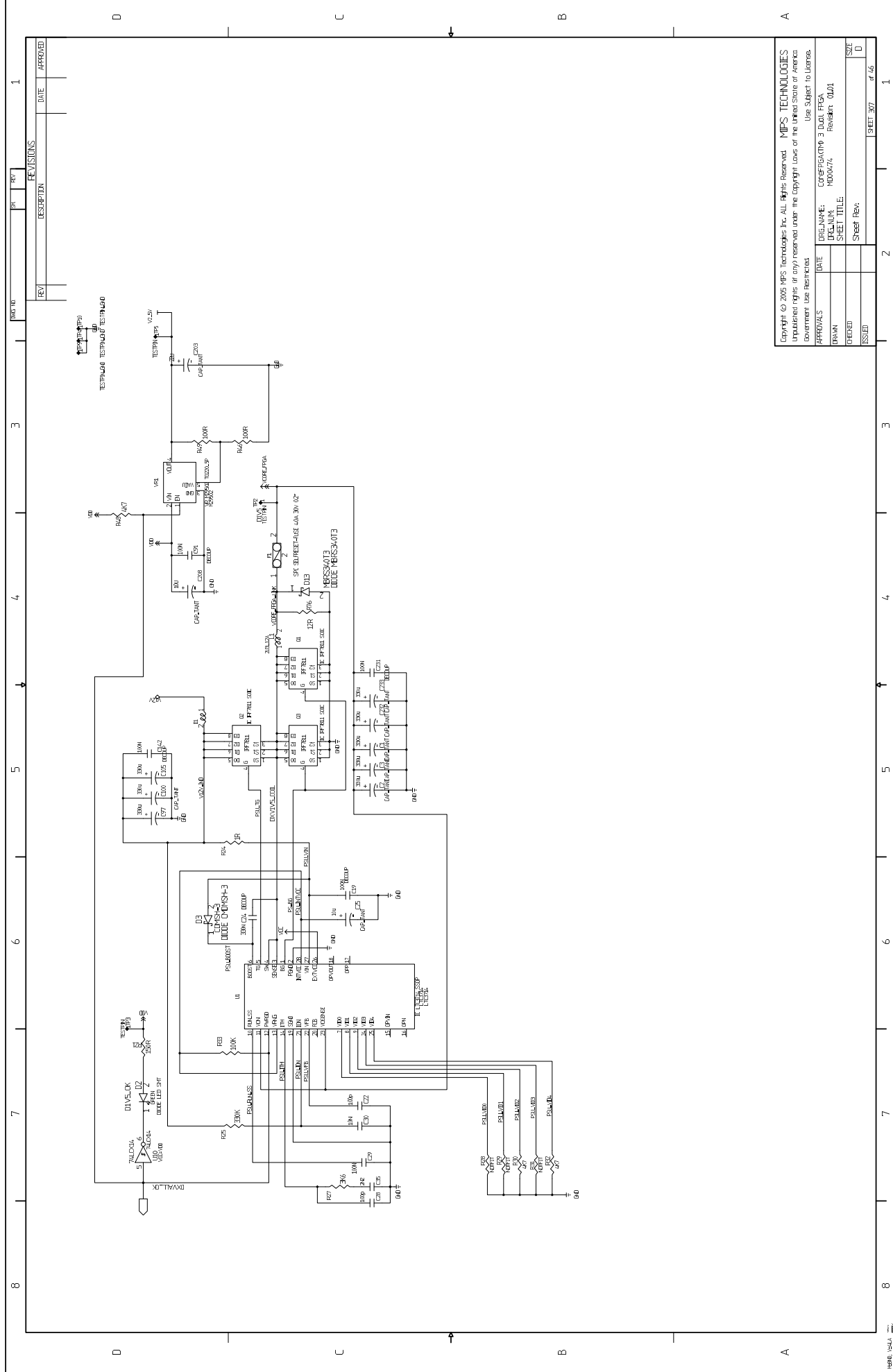


REV	DESCRIPTION	DATE	APPROVED

APPROVALS	
DATE	DESIGNER
CHECKED	DESIGNER
ISSUED	DESIGNER

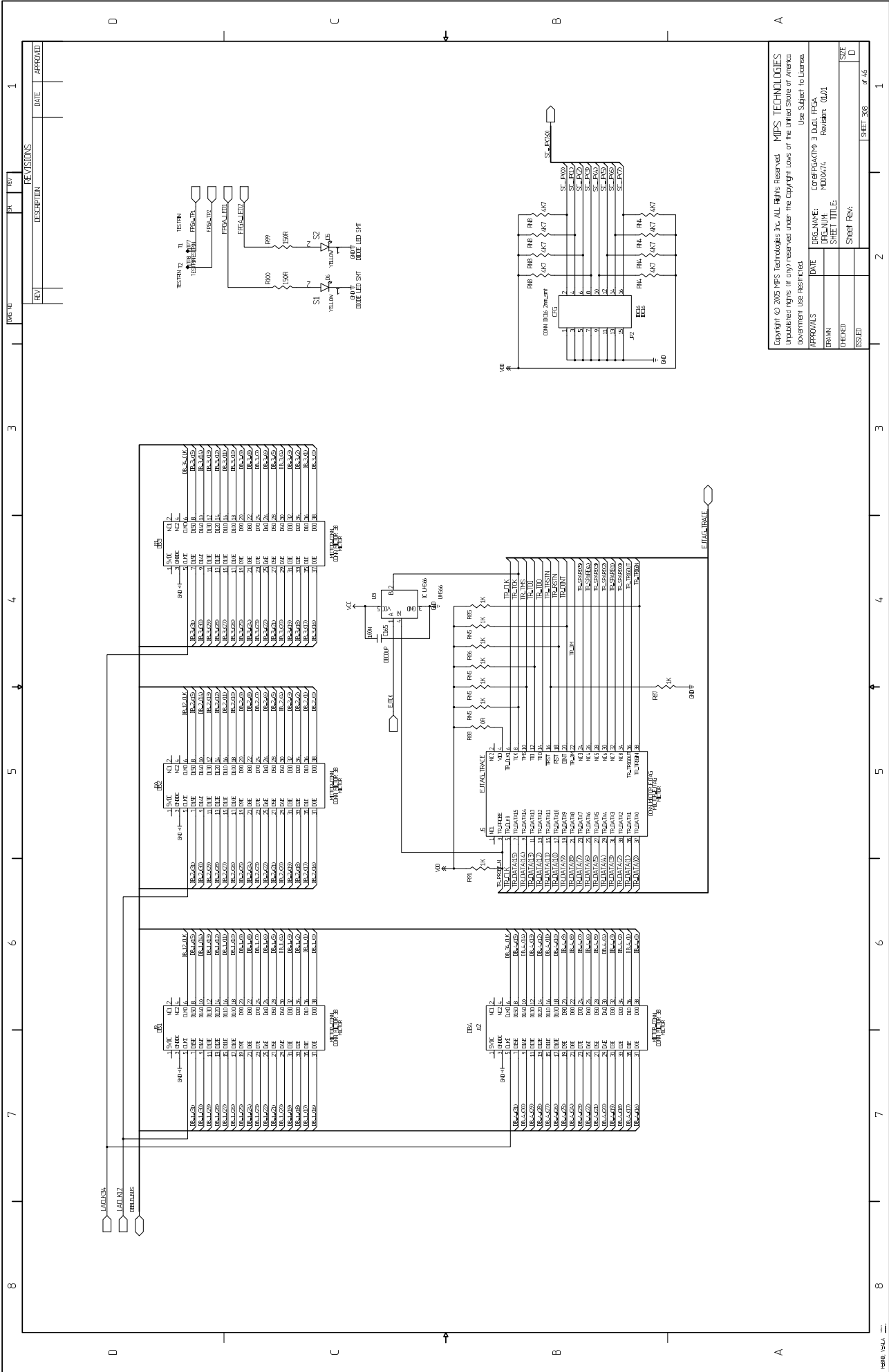
PROJECT NAME: COSEFACTING 3 DUAL FPGA
 PROJECT NO: H000074
 SHEET TITLE: BOARDKIT_0001
 SHEET REV: 1
 SHEET 306 of 46

Copyright © 2005 MIPS Technologies, Inc. All Rights Reserved. MIPS TECHNOLOGIES
 Unpublished rights (if any) reserved under the Copyright Laws of the United States of America.
 Government Use Restricted. Use Subject to License.



REV	DESCRIPTION	DATE	APPROVED

APPROVALS		MIPS TECHNOLOGIES	
DATE	DESIGNER	DATE	DESIGNER
CHECKED	DESIGNED	DATE	DESIGNER
ISSUED	DESIGNED	DATE	DESIGNER



REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

APPROVALS	
DATE	DESIGNER
CHECKED	DESIGNER
ISSUED	DESIGNER

MIPS TECHNOLOGIES	
DATE	DESIGNER
CHECKED	DESIGNER
ISSUED	DESIGNER

MIPS TECHNOLOGIES	
DATE	DESIGNER
CHECKED	DESIGNER
ISSUED	DESIGNER

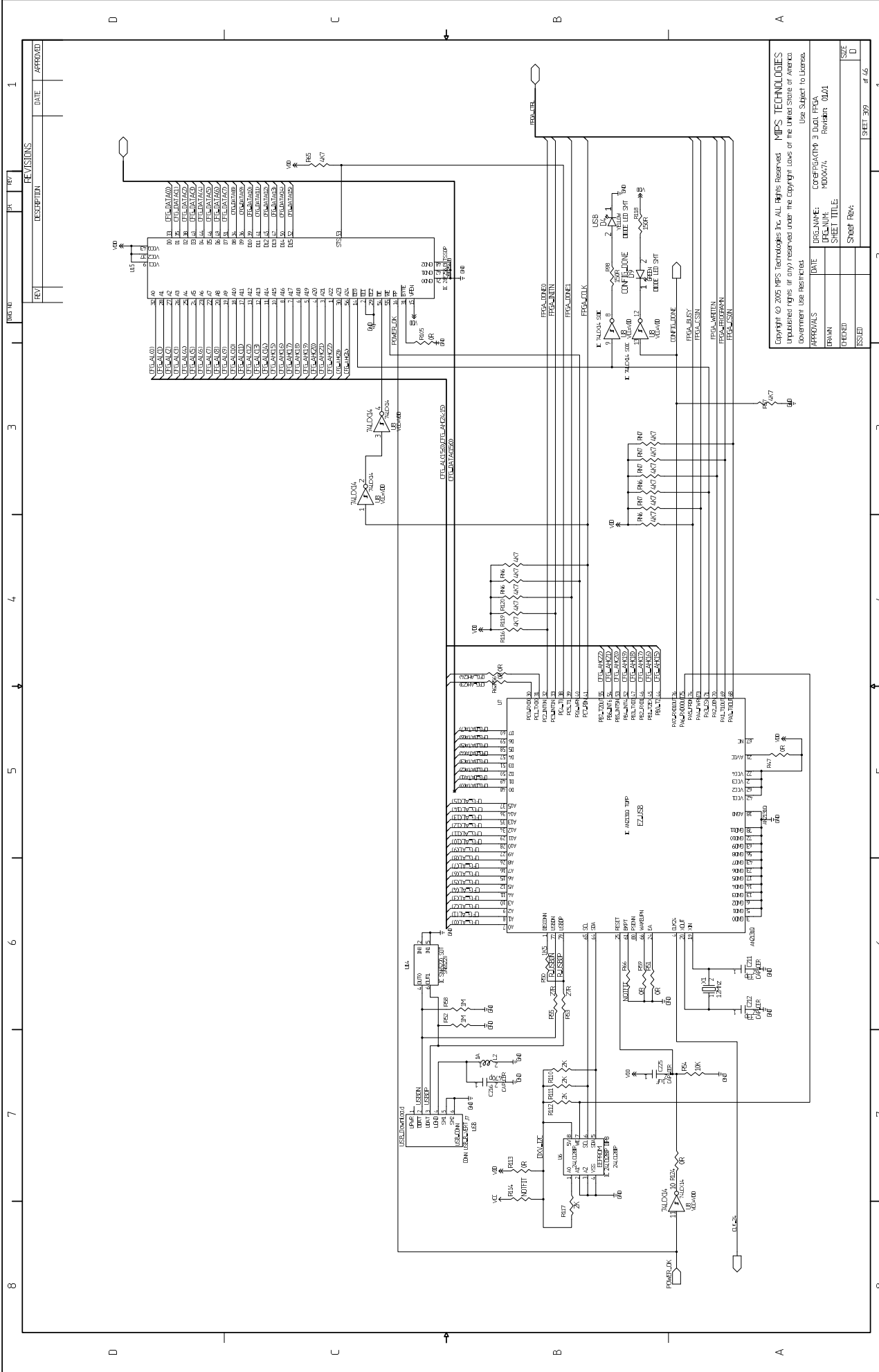
MIPS TECHNOLOGIES	
DATE	DESIGNER
CHECKED	DESIGNER
ISSUED	DESIGNER

MIPS TECHNOLOGIES	
DATE	DESIGNER
CHECKED	DESIGNER
ISSUED	DESIGNER

MIPS TECHNOLOGIES	
DATE	DESIGNER
CHECKED	DESIGNER
ISSUED	DESIGNER

MIPS TECHNOLOGIES	
DATE	DESIGNER
CHECKED	DESIGNER
ISSUED	DESIGNER

MIPS TECHNOLOGIES	
DATE	DESIGNER
CHECKED	DESIGNER
ISSUED	DESIGNER



REV	DESCRIPTION	DATE	APPROVED

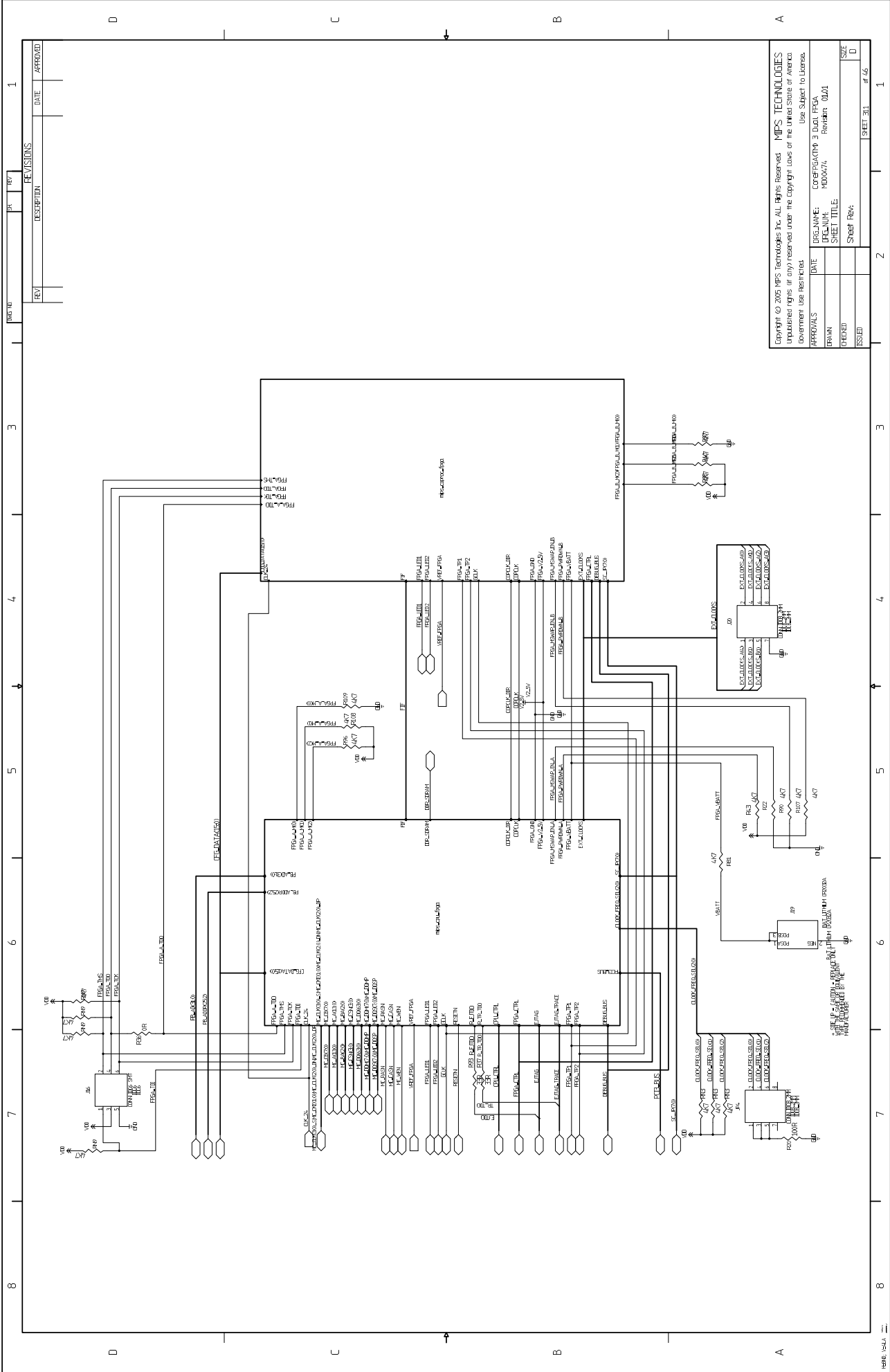
REV	DESCRIPTION	DATE	APPROVED

Copyright © 2005 MIPS Technologies, Inc. All Rights Reserved.
 Unpublished rights reserved under the Copyright Laws of the United States of America.
 Government Use Restricted. Use Subject to License.

DATE: 11/03/05
 Dwg Name: CORE/FPGA3 DUAL FPGA
 Dwg No: 10000474
 Sheet Title: BoardKit_0001

APPROVALS
 DRAWN: [Signature]
 CHECKED: [Signature]
 ISSUED: [Signature]

Sheet Rev: []
 SIZE: D
 SHEET 309 of 46



REV	DESCRIPTION	DATE	APPROVED

APPROVALS		DATE	DESIGN NAME

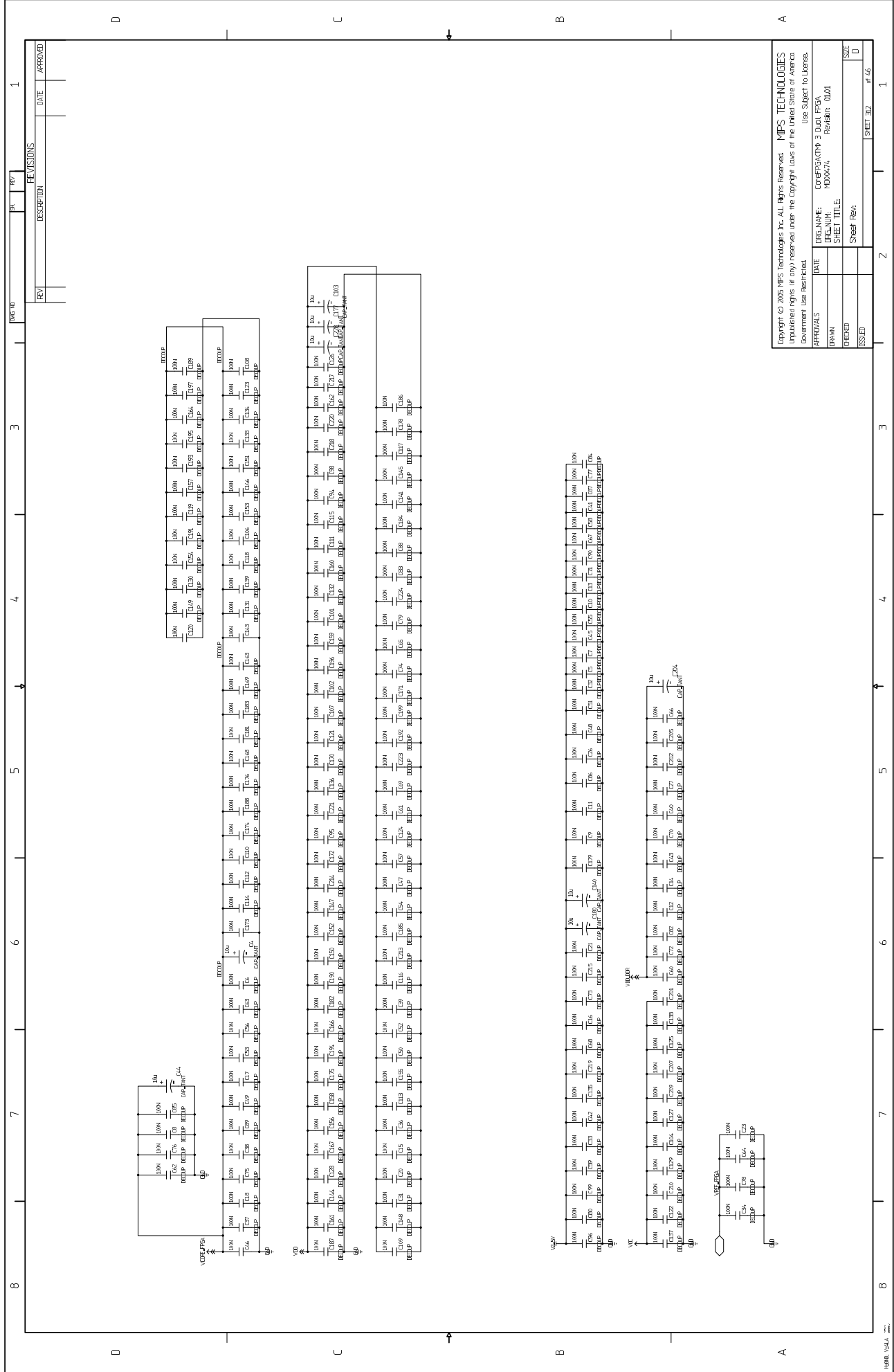
REV	DESCRIPTION	DATE	APPROVED

Copyright © 2005 MIPS Technologies, Inc. All Rights Reserved. MIPS TECHNOLOGIES
 Unpublished rights (if any) reserved under the Copyright Laws of the United States of America
 Government Use Restricted

APPROVALS

DESIGN NAME: COFFEINATING 3 DUAL FPGA
 DCL NUM: H000074
 SHEET TITLE: BoardKit_0001

DRAWN: Sheet Rev: SIZE: D
 CHECKED: ISSUED: SHEET 31 of 46



REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

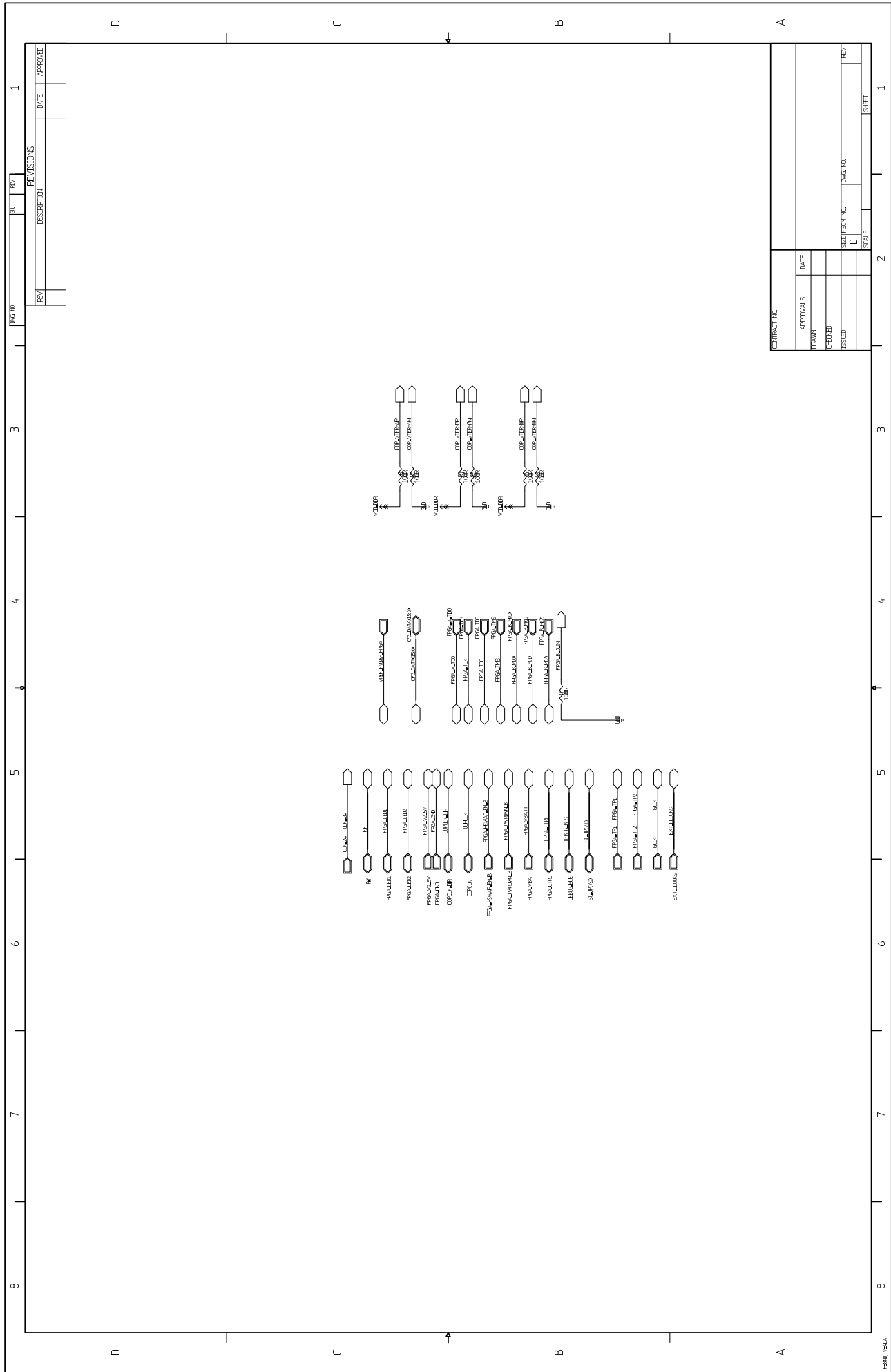
Copyright © 2005 MIPS Technologies, Inc. All Rights Reserved. MIPS TECHNOLOGIES
 Unpublished rights: (if any) reserved under the Copyright Laws of the United States of America
 Government Use Restricted

APPROVALS

DATE	DESIGNER	DESIGN TITLE	SIZE

DRAWN	CHECKED	ISSUED

CONFIDENTIAL
 SHEET TITLE: SHEET 32 of 46



REV. NO. PART NO. REV. NO.

REV.	DESCRIPTION	DATE	APPROVED

CONTRACT NO.

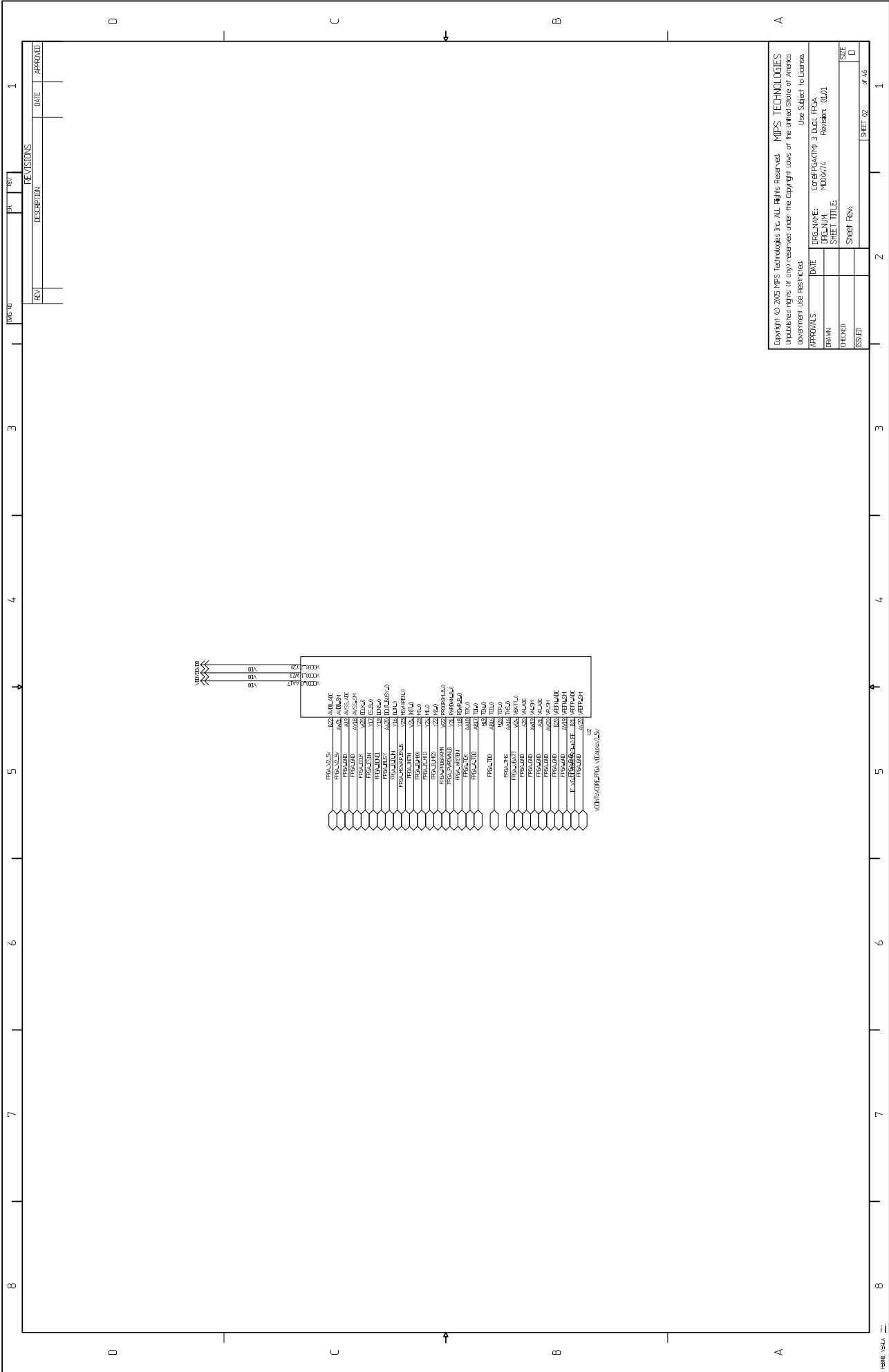
APPROVALS	DATE
DESIGN	
CHECKED	
TESTED	

SHEET NO. 0

DATE: 12/14/05

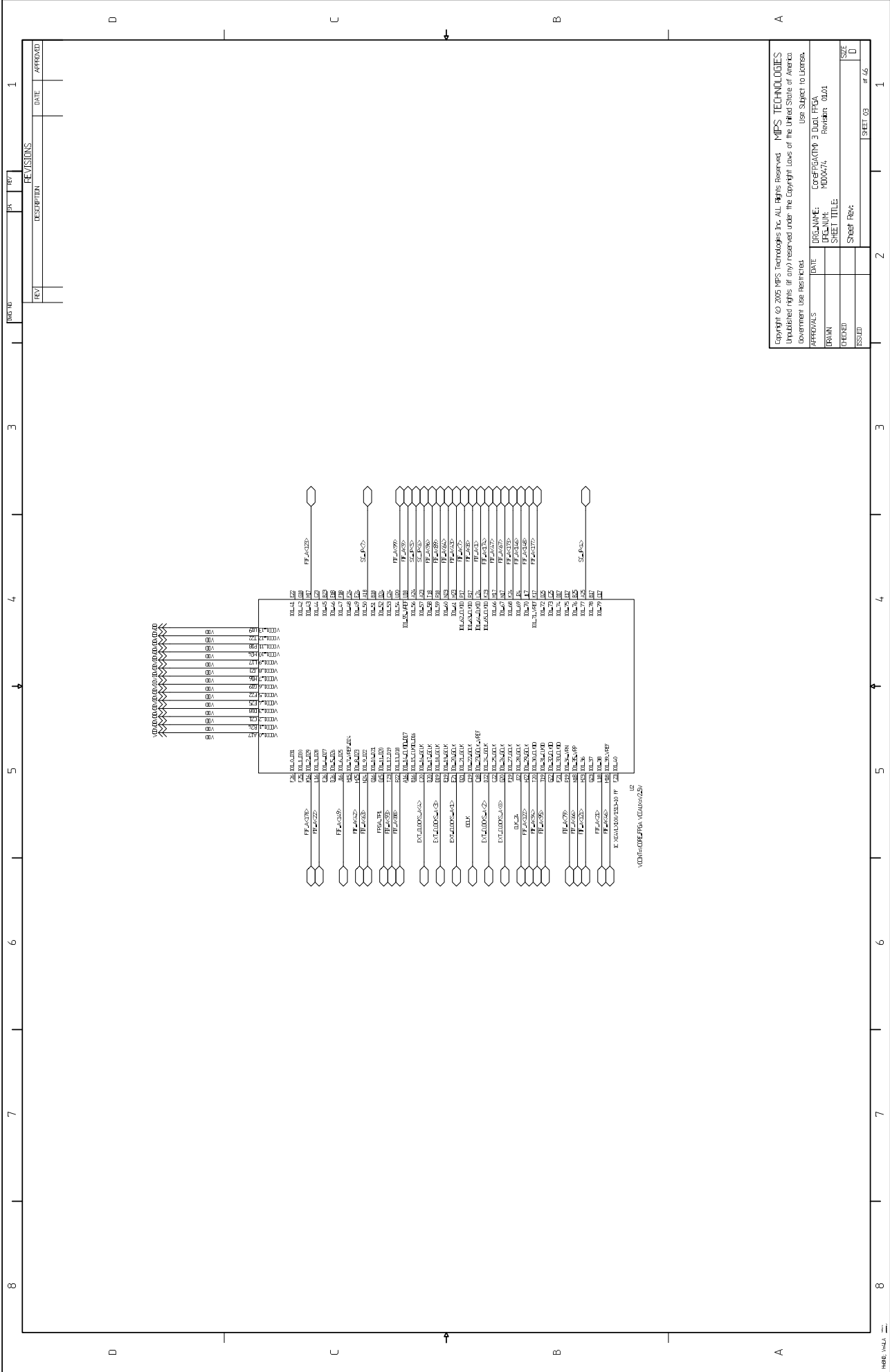
SCALE

SHEET 1



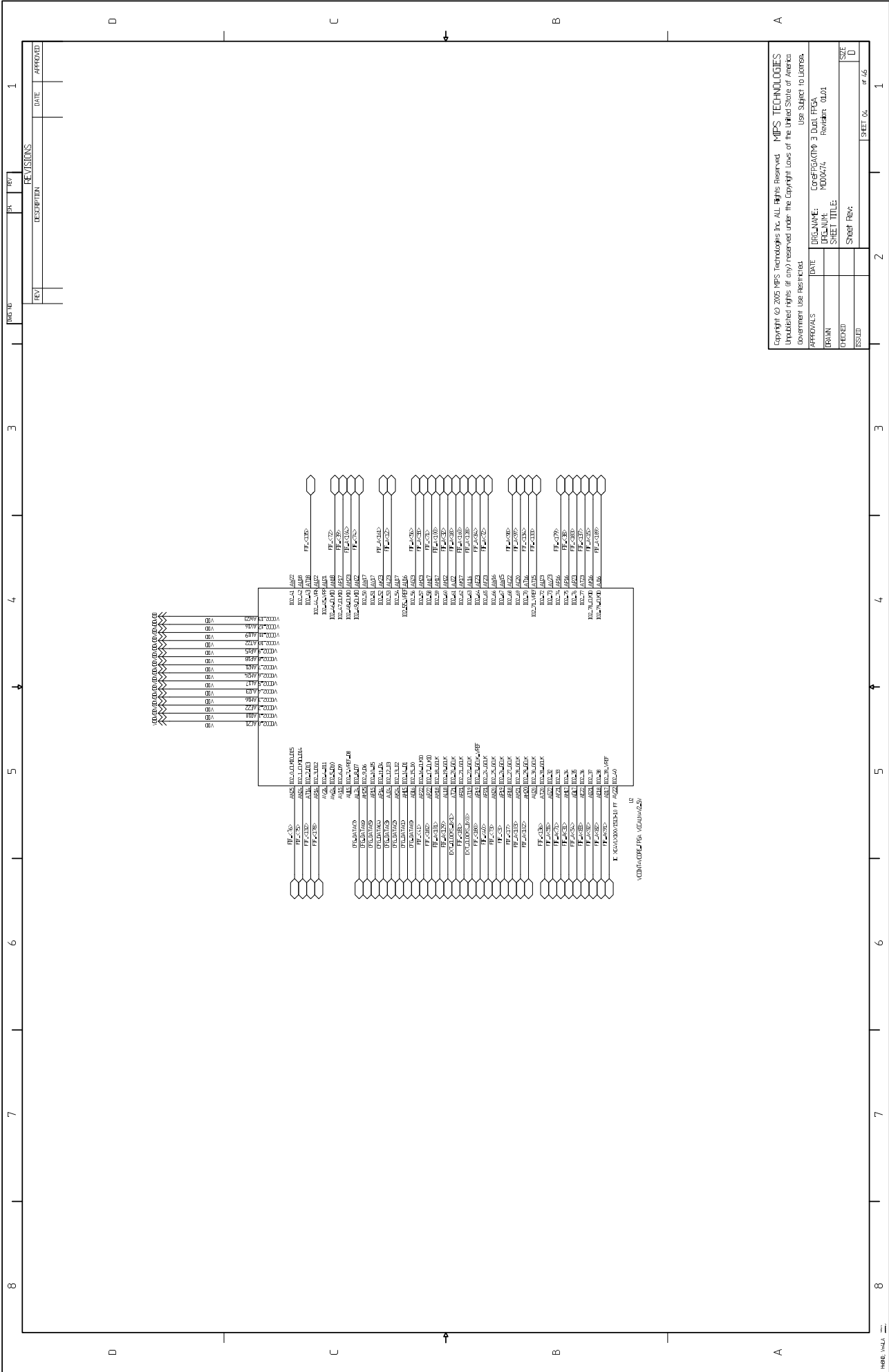
REV	DESCRIPTION	DATE	APPROVED

Copyright © 2005 MIPS Technologies, Inc. All Rights Reserved. MIPS TECHNOLOGIES Unpublished rights (if any) reserved under the Copyright Laws of the United States of America. Government Use Restricted. Use Subject to License.	
DATE	02/01/05
DESIGNER	COSE/STANISLAW
DRAWN	H000074
CHECKED	
ISSUED	
SHEET TITLE	
Sheet No.	001
Sheet Rev.	
SIZE	D
SHEET 02	of 06



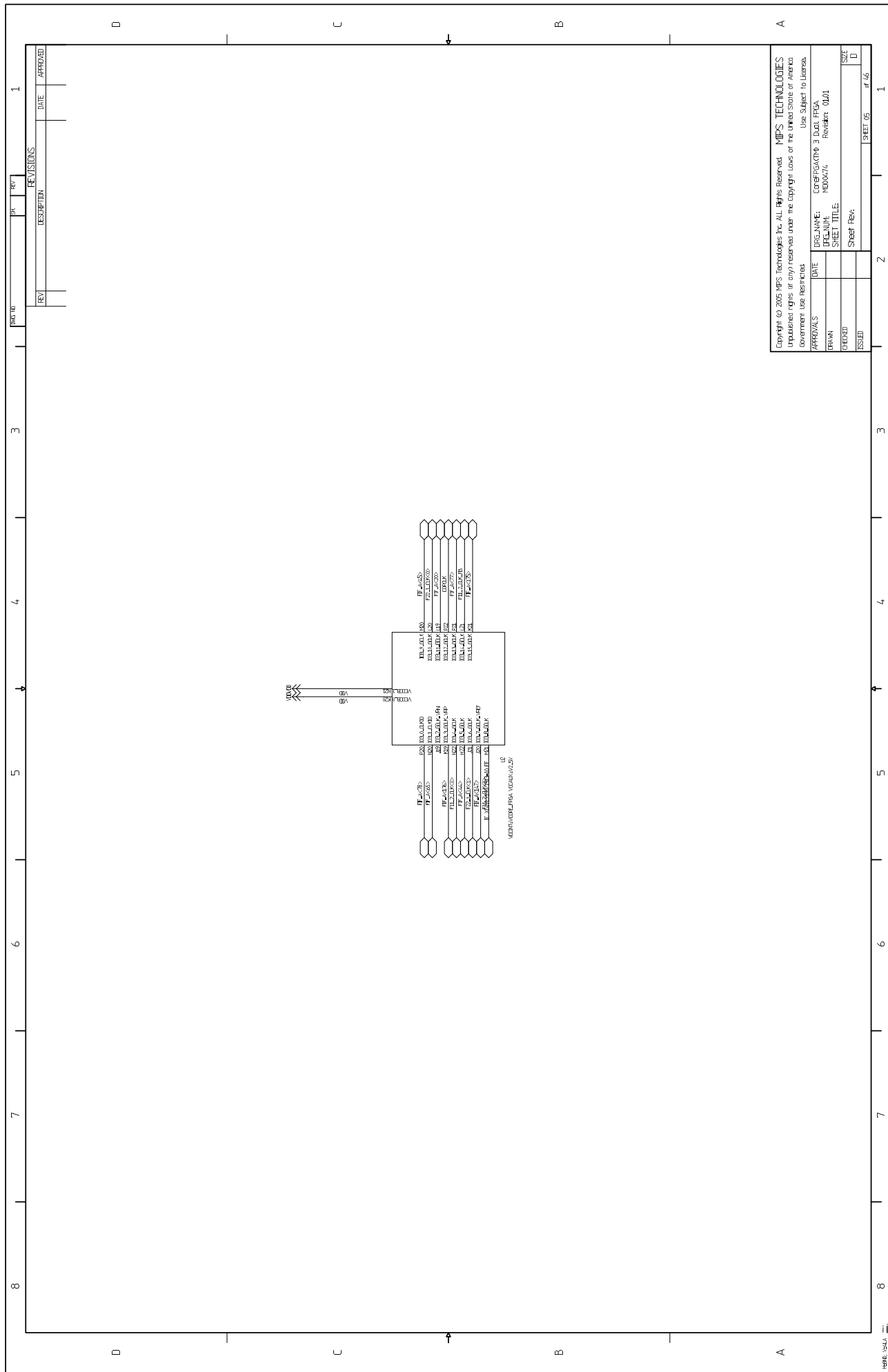
REV	DESCRIPTION	DATE	APPROVED

Copyright © 2005 MIPS Technologies, Inc. All Rights Reserved. MIPS TECHNOLOGIES Unpublished MIPS (if any) reserved under the Copyright Laws of the United States of America. Government Use Restricted. Use Subject to License.	
DATE	
DWG. NAME	COEFFICIENT 3 Dual FPGA
DWG. NO.	1000474
SHEET TITLE	Reboard: 0101
DRAWN	
CHECKED	
ISSUED	
Sheet No.	
Sheet Rev.	
SIZE	D
SHEET 03	of 06



REV	DESCRIPTION	DATE	APPROVED

Copyright © 2005 MIPS Technologies, Inc. All Rights Reserved. MIPS TECHNOLOGIES Unpublished MIPS (if any) reserved under the Copyright Laws of the United States of America. Government Use Restricted.	
DATE	COEFFICIENT 3 Dual FPGA
DRAWN	10000474
CHECKED	10000474
ISSUED	10000474
SHEET	04
OF	06

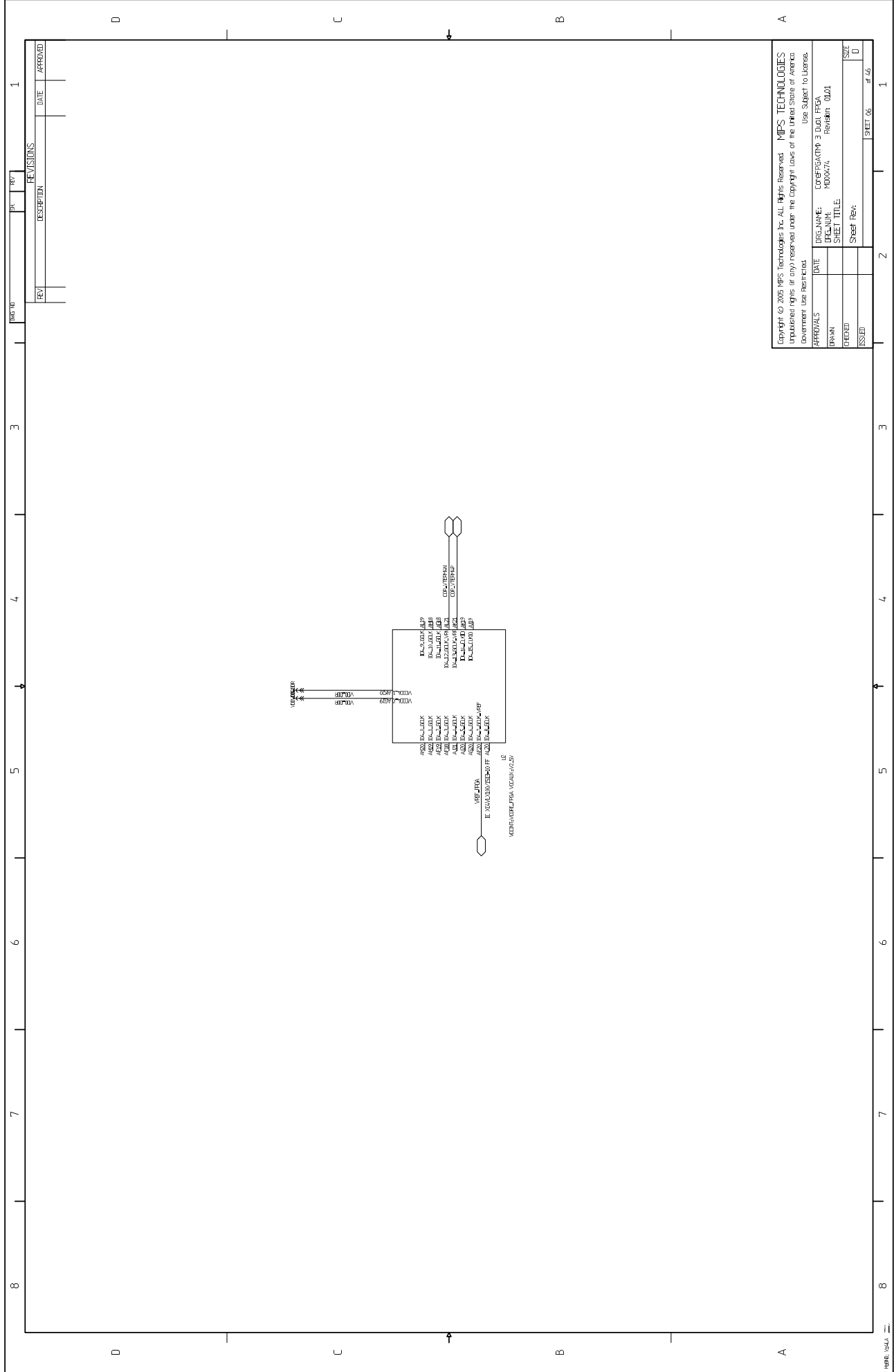


REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

DATE	DESIGNER	DRAWN	CHECKED	ISSUED	SHEET	REV

Copyright © 2005 MIPS Technologies, Inc. All Rights Reserved. MIPS TECHNOLOGIES
 Unpublished rights (if any) reserved under the Copyright Laws of the United States of America
 Government Use Restricted Use Subject to License

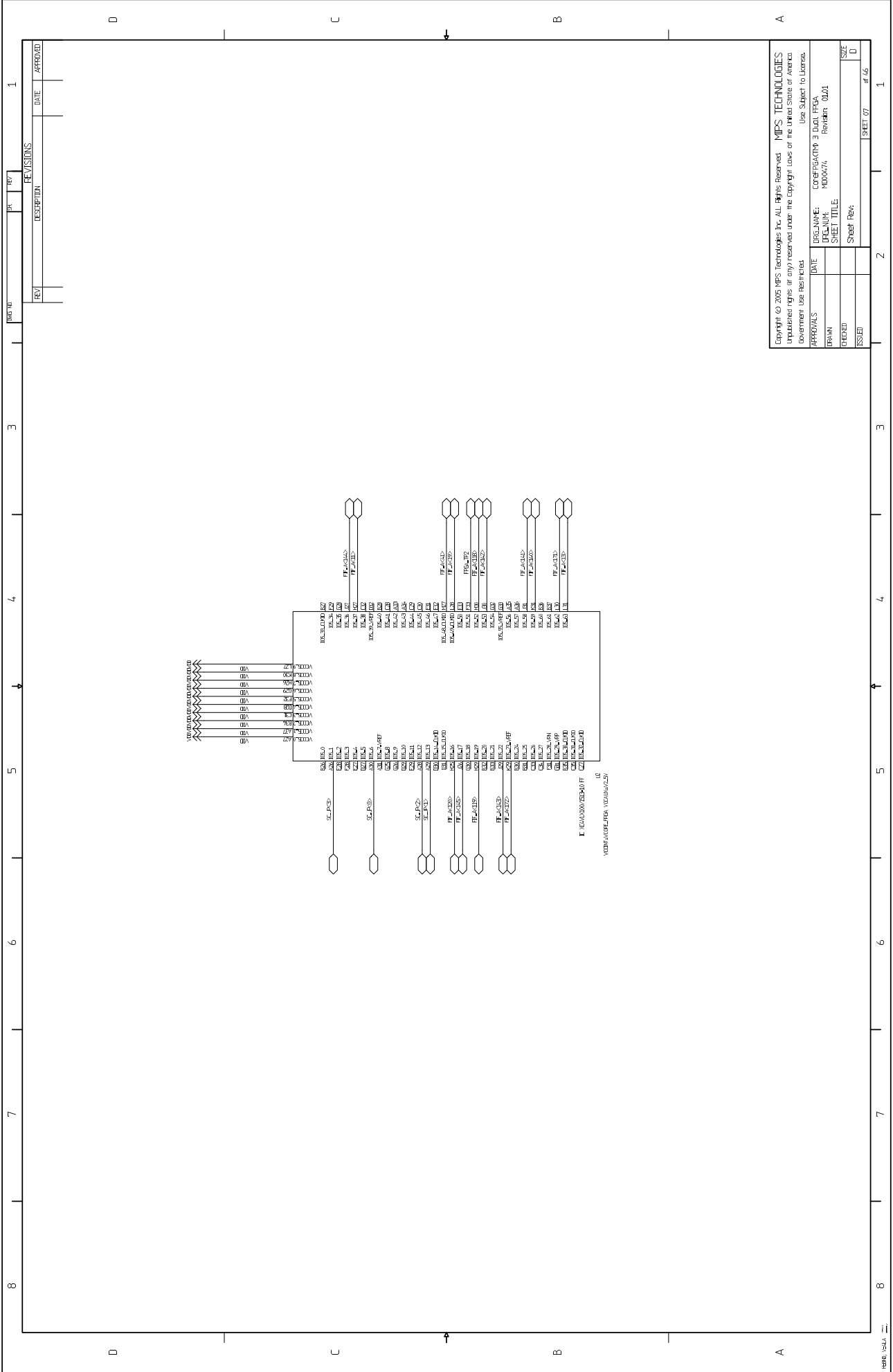
DATE: 10/06/05
 DESIGNER: COOPERATING 3 DUAL FPGA
 DRAWN: H000074
 CHECKED: H000074
 ISSUED: H000074
 SHEET: 05 of 06
 REV: D



REV	DESCRIPTION	DATE	APPROVED

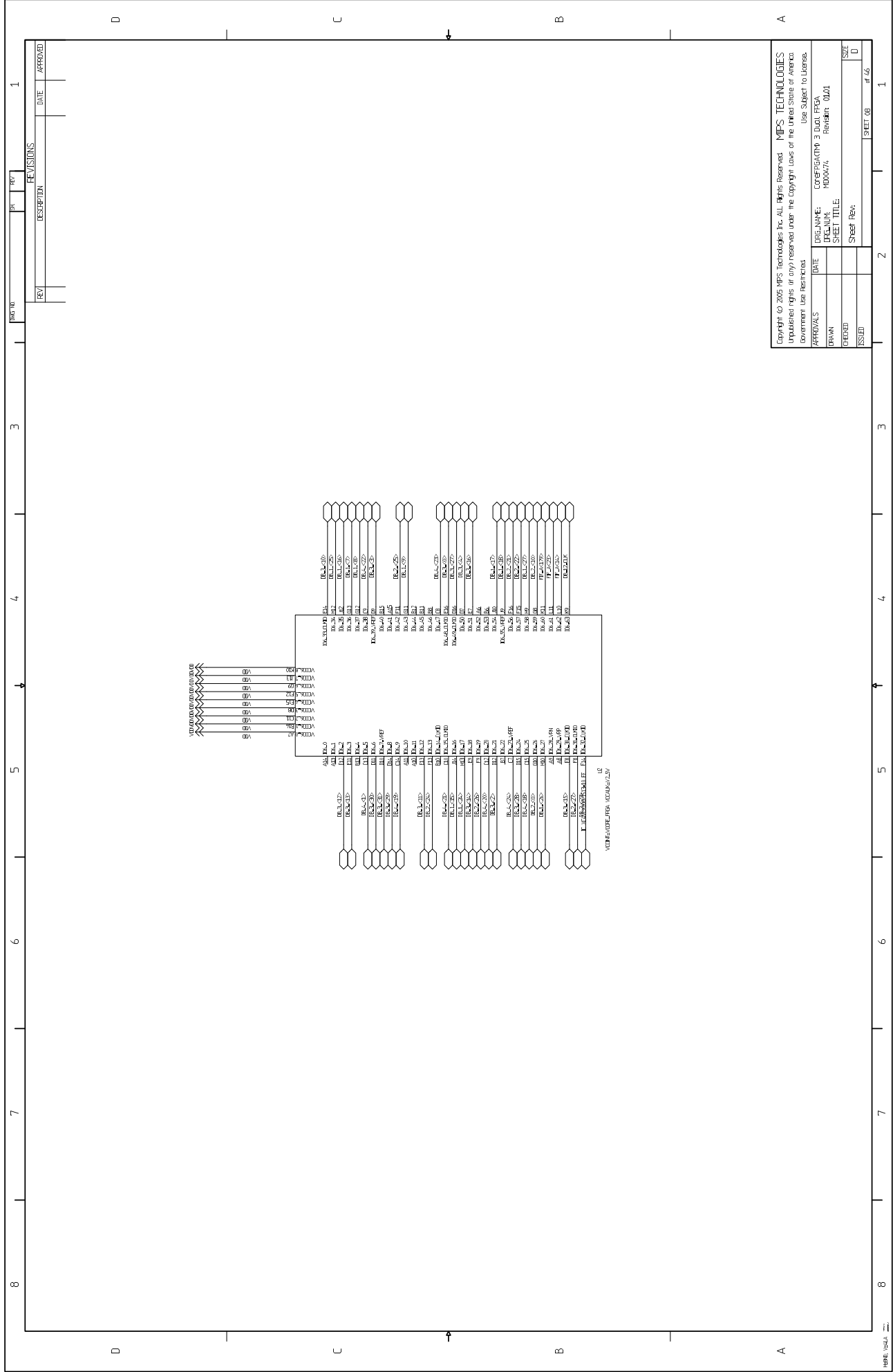
APPROVALS		DATE	DESIGN NAME	PROJECT NAME	DESIGN NO.	REV	DATE	APPROVED
DRAWN	CHECKED	ISSUED	II_VGA1024X768_V01	II_VGA1024X768_V01	10000076	0001		

Copyright © 2005 MIPS Technologies, Inc. All Rights Reserved. MIPS TECHNOLOGIES
 Unpublished rights (if any) reserved under the Copyright Laws of the United States of America
 Government Use Restricted Use Subject to License



REV	DESCRIPTION	DATE	APPROVED

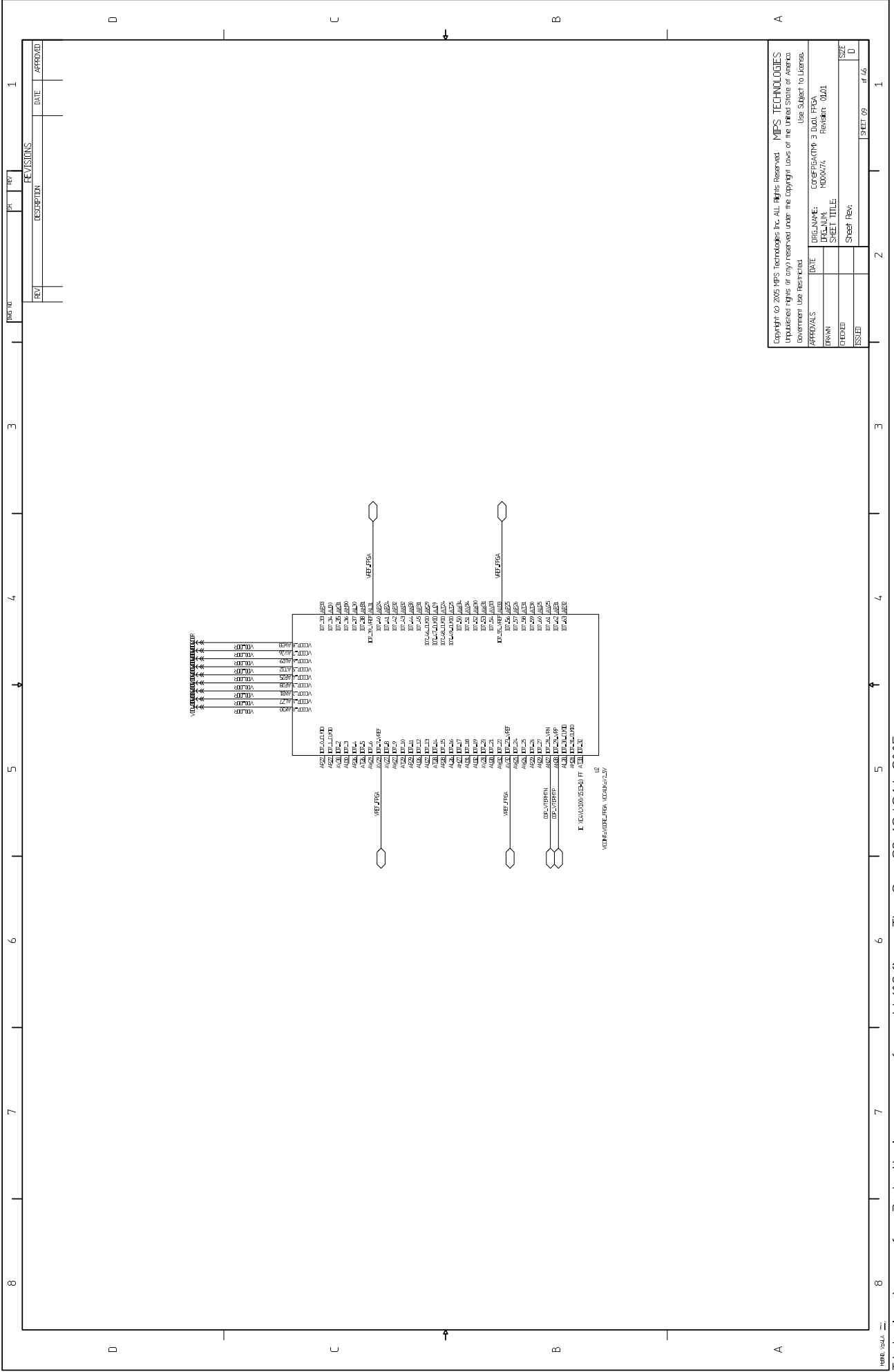
Copyright © 2005 MIPS Technologies, Inc. All Rights Reserved. MIPS TECHNOLOGIES Unpublished rights: (if any) reserved under the Copyright Laws of the United States of America Government Use Restricted Use Subject to License	
DATE	
DESIGNER	
CHECKED	
ISSUED	
DRAWN	
DATE	
DESIGN NAME	COREFPGA3P3 Dual FPGA
DRAWING NO.	10000074
SHEET TITLE	Block 001
Sheet No.	07 of 46
SIZE	D



REV	DESCRIPTION	DATE	APPROVED

REV		REV		REV	
NO	NO	NO	NO	NO	NO

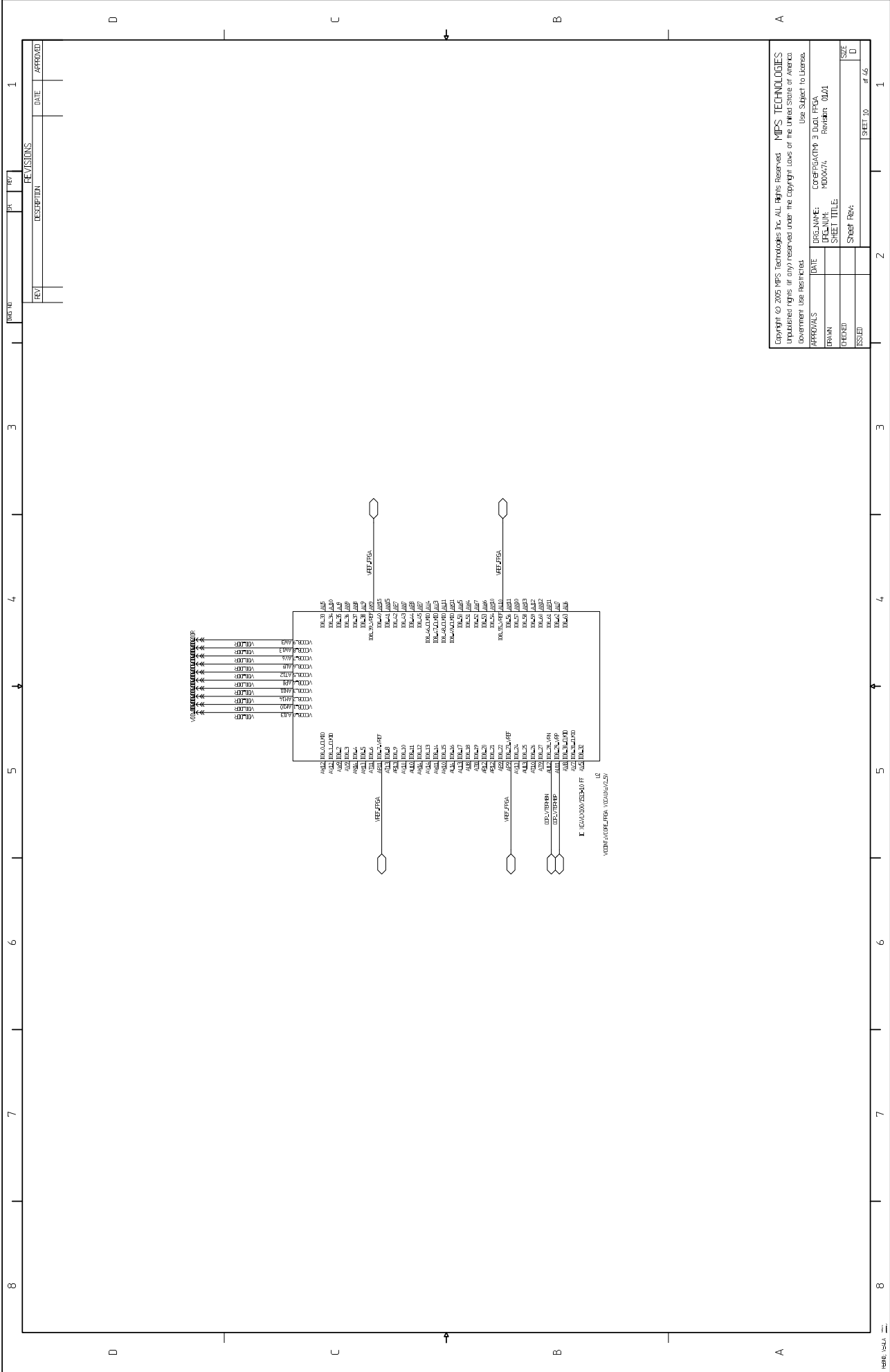
Copyright © 2005 MIPS Technologies, Inc. All Rights Reserved. MIPS TECHNOLOGIES Unpublished rights (if any) reserved under the Copyright Laws of the United States of America. Government Use Restricted. Use Subject to License.					
DATE		DESIGNER			
CHECKED		DRAWN			
ISSUED		SHEET	08	of	06
		SHEET TITLE			
		PROJECT			



REV	DESCRIPTION	DATE	APPROVED

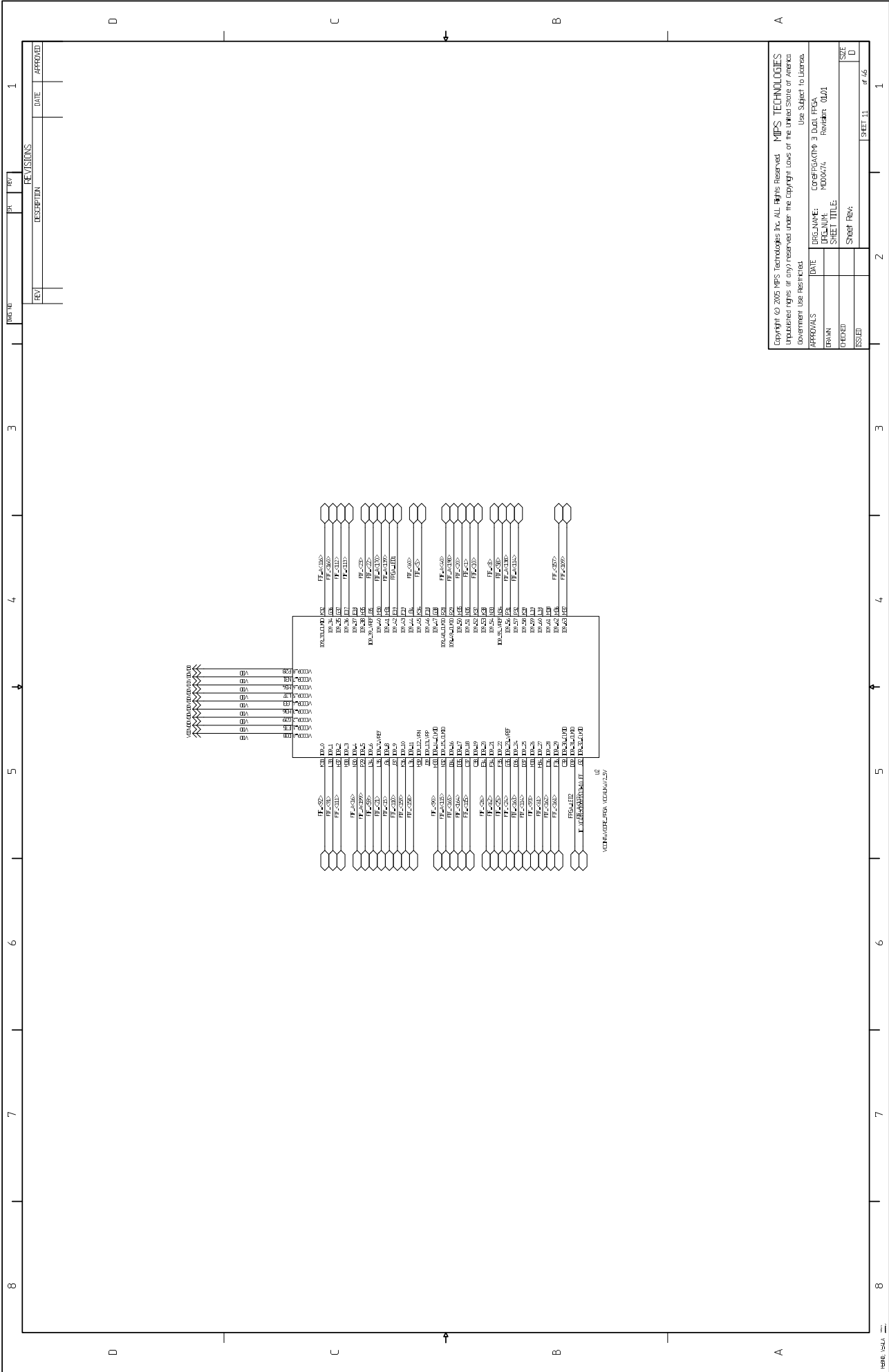
REV	DESCRIPTION	DATE	APPROVED

Copyright © 2005 MIPS Technologies, Inc. All Rights Reserved. MIPS TECHNOLOGIES
Unpublished Rights: (if any) reserved under the Copyright Laws of the United States of America.
Government Use Restricted. Use Subject to License.
APPROVALS: DATE: COSMOS/CMO 3 DUAL FPGA
DRAWN: SHEET NAME: H0000474 Revision: 0.001
CHECKED: SHEET TITLE: Sheet Rev: D
ISSUED: SHEET 09 of 06



REV	DESCRIPTION	DATE	APPROVED

Copyright © 2005 MIPS Technologies, Inc. All Rights Reserved. MIPS TECHNOLOGIES Unpublished rights (if any) reserved under the Copyright Laws of the United States of America. Government Use Restricted. Use Subject to License.	
DESIGN NAME:	COREFACING 3 DUAL FPGA
DRAWN:	H000074
CHECKED:	
ISSUED:	
SHEET TITLE:	
Sheet No.:	
Sheet Rev.:	
SIZE:	D
SHEET 10	of 16

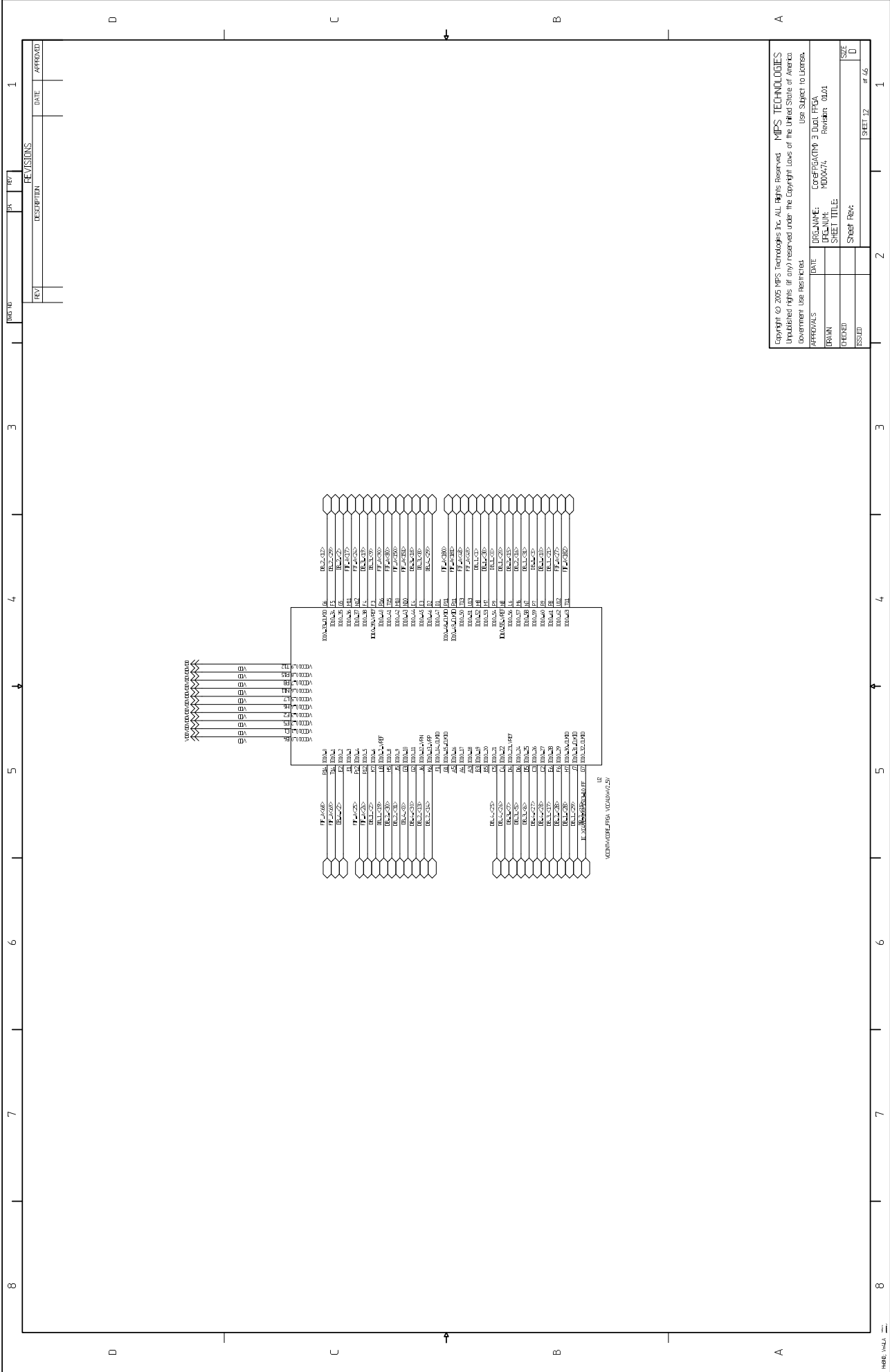


REV	DESCRIPTION	DATE	APPROVED

APPROVALS		DATE	DESIGN NAME	DATE	DESIGN NAME
DRAWN	CHECKED	ISSUED			

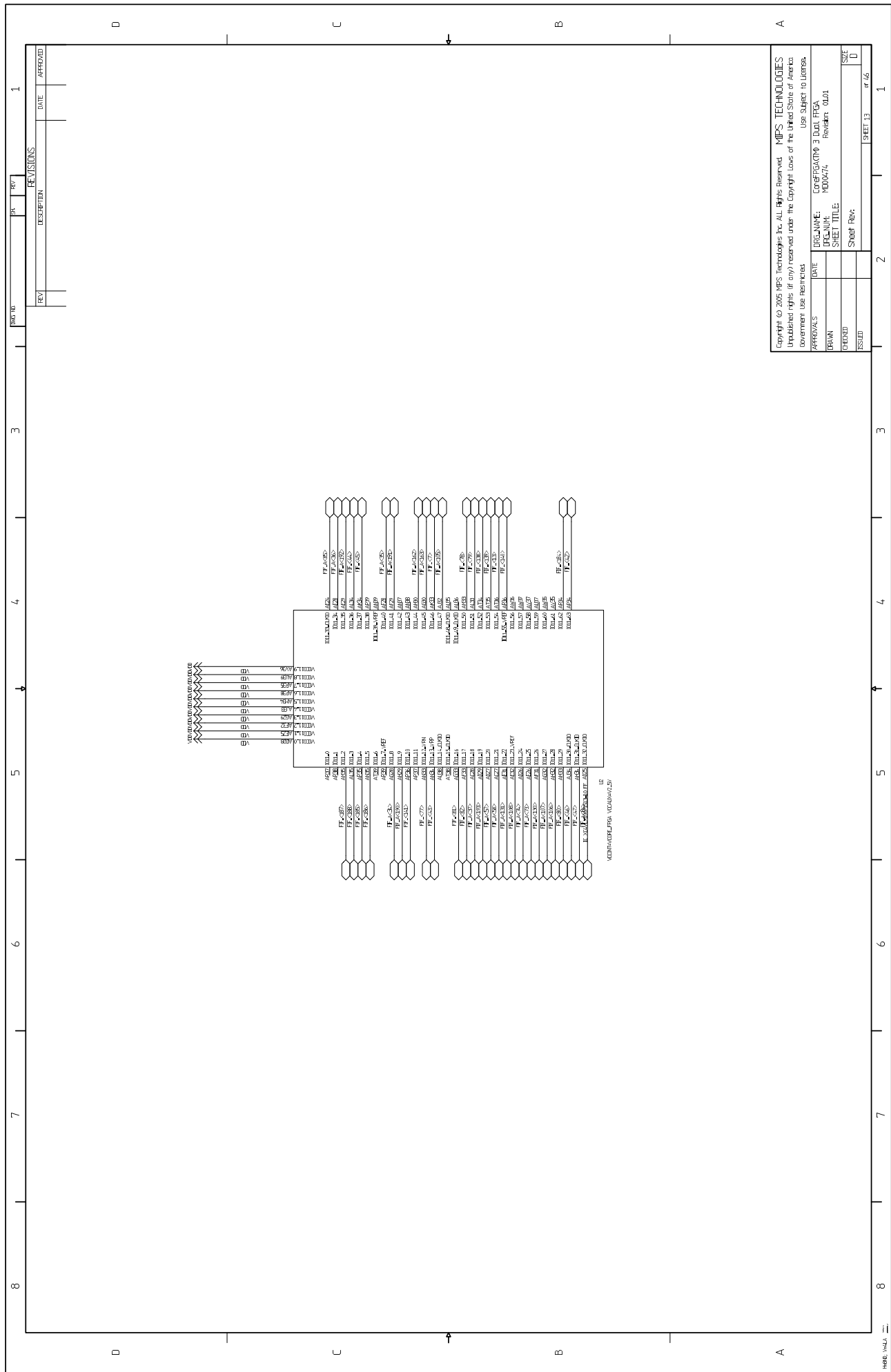
Copyright © 2005 MIPS Technologies, Inc. All Rights Reserved. MIPS TECHNOLOGIES
 Unpublished rights (if any) reserved under the Copyright Laws of the United States of America.
 Government Use Restricted. Use Subject to License.

COOPERATING 3 DUAL FPGA
 H000074
 SHEET TITLE: BoardKit_0001
 Sheet Rev: 0
 SIZE: D
 SHEET 11 of 16



REV	DESCRIPTION	DATE	APPROVED

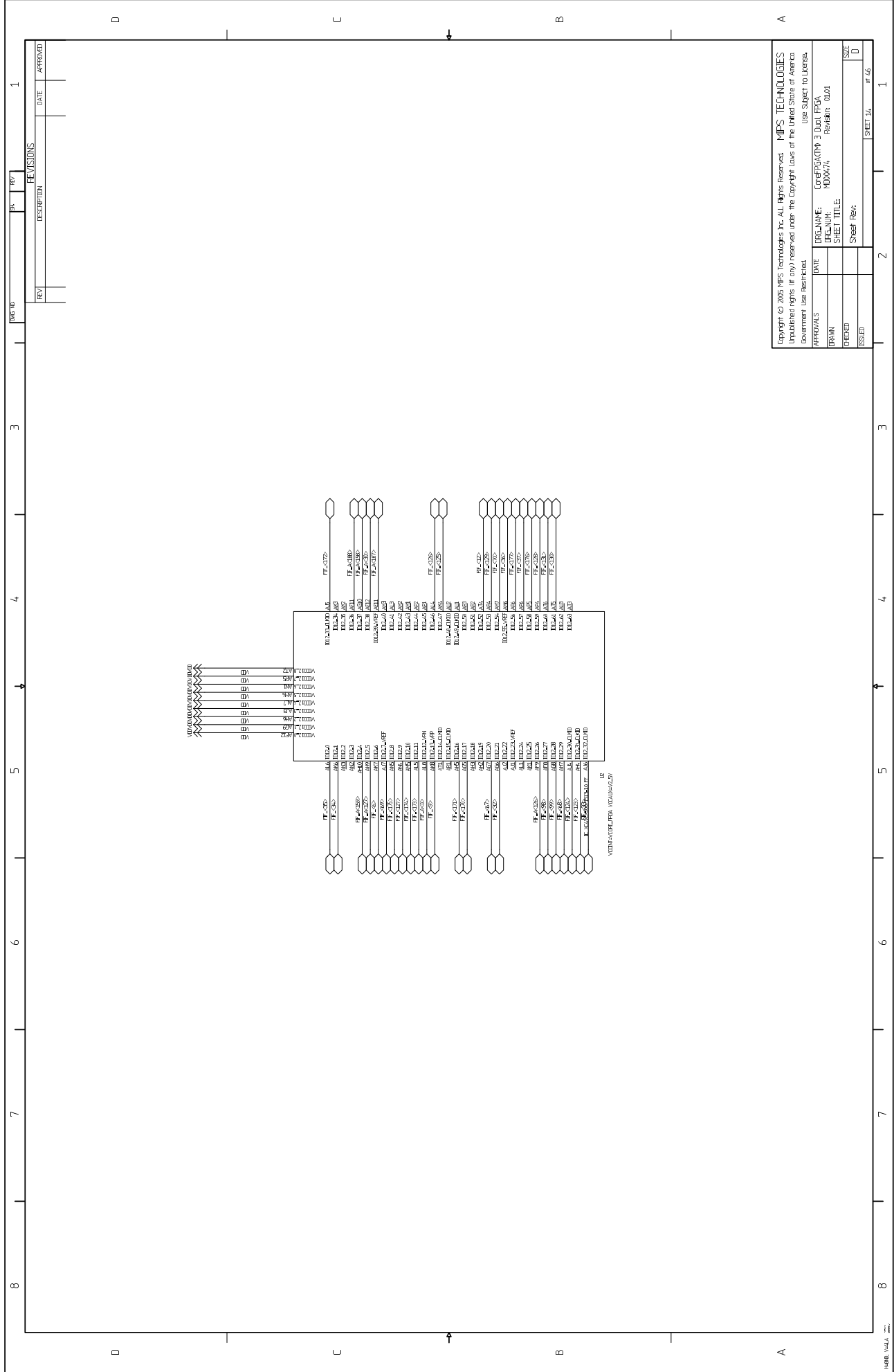
Copyright © 2005 MIPS Technologies, Inc. All Rights Reserved. MIPS TECHNOLOGIES Unpublished MIPS (if any) reserved under the Copyright Laws of the United States of America. Government Use Restricted.	
DATE	COSERVATING 3 Dual FPGA
DWG NAME	100A.1100
SHEET TITLE	Revision: 0.0.1
CHECKED	Sheet Rev:
ISSUED	SHEET 12 of 46



UR
V001140646/P0A_V000000425P

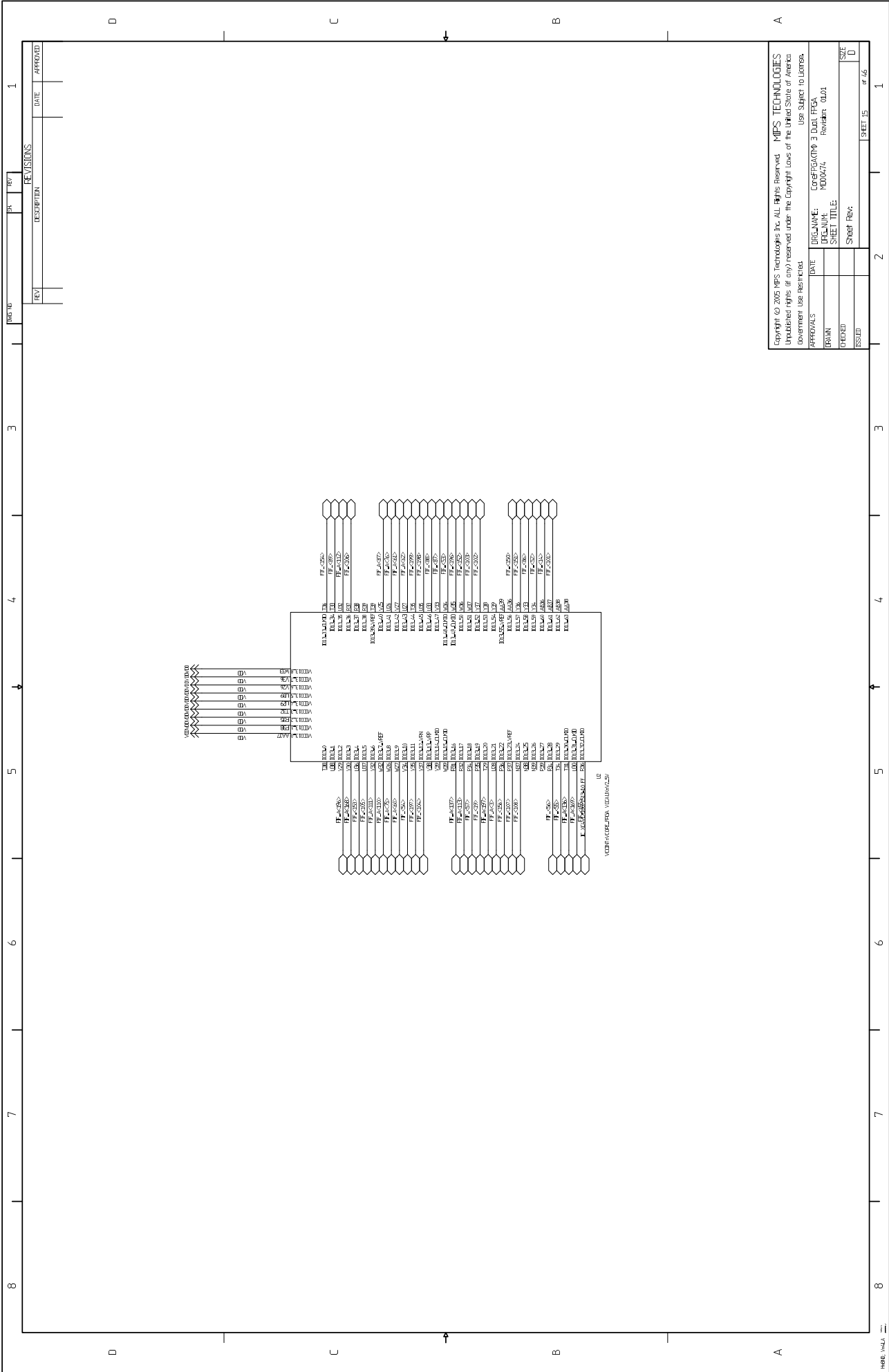
REV	REV	REV	REV	REV	REV	REV	REV	REV	REV
REVISIONS									
	REV	DESCRIPTION	DATE	APPROVED					

Copyright © 2005 MIPS Technologies, Inc. All Rights Reserved. MIPS TECHNOLOGIES Unpublished MIPS (if any) reserved under the Copyright Laws of the United States of America. Government Use Restricted. Use Subject to License.				
DATE	DESIGNER	CHECKED	ISSUED	SIZE
	10/04/05			D
DRAWN		SHEET 13 OF 16		
PROJECT		PROJECT TITLE		
DESIGN NAME		SHEET No.		
DRAWING No.		Sheet Rev.		



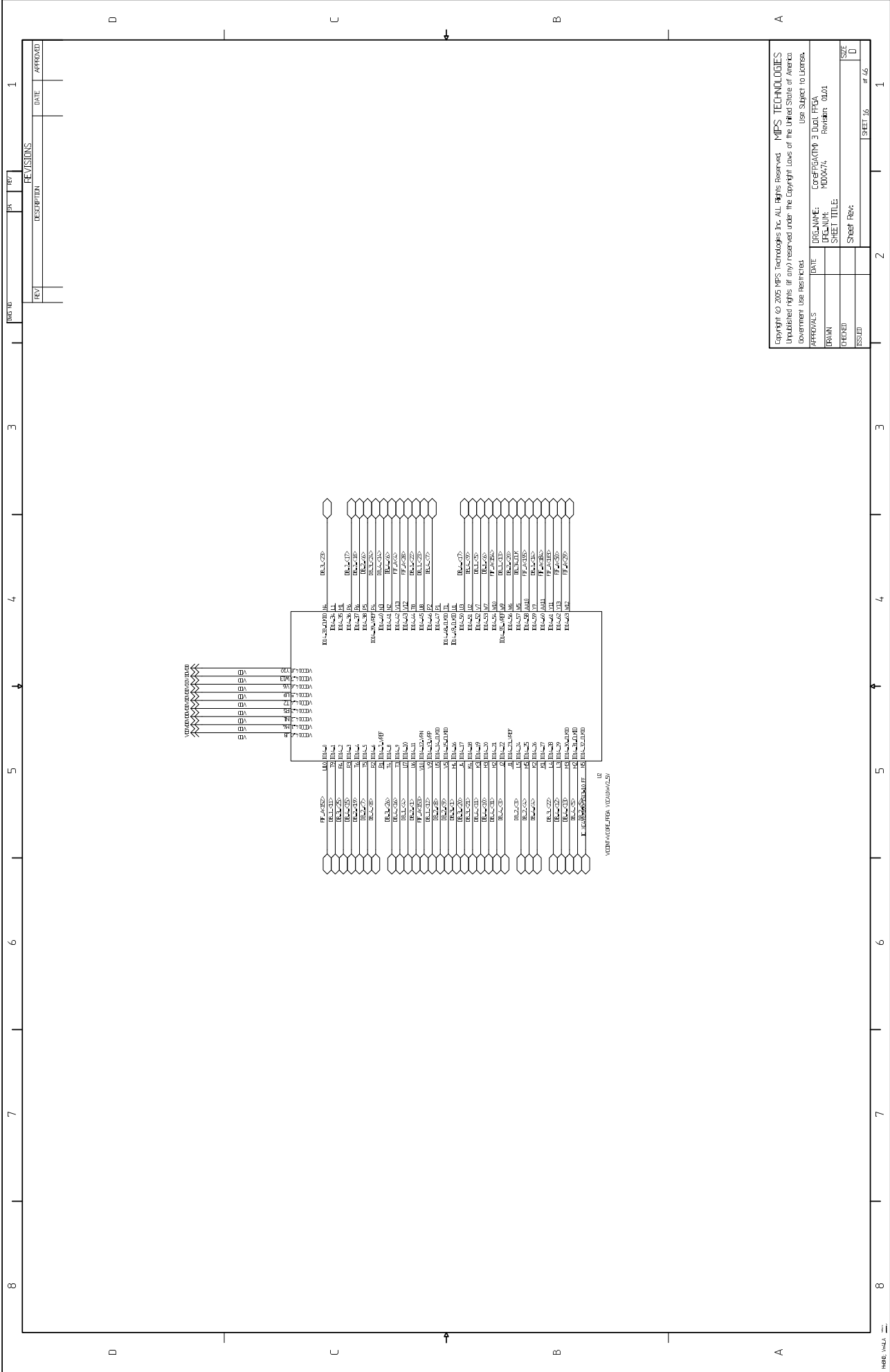
REV	DESCRIPTION	DATE	APPROVED

Copyright © 2005 MIPS Technologies, Inc. All Rights Reserved. MIPS TECHNOLOGIES Unpublished MIPS (if any) reserved under the Copyright Laws of the United States of America. Government Use Restricted.	
DATE	COEFFICIENT 3 Dual FPGAs
DWG NAME	10000474
DRAWN	Revised: 01/01
CHECKED	
ISSUED	
Sheet No.	SHEET 14 of 16
SIZE	D



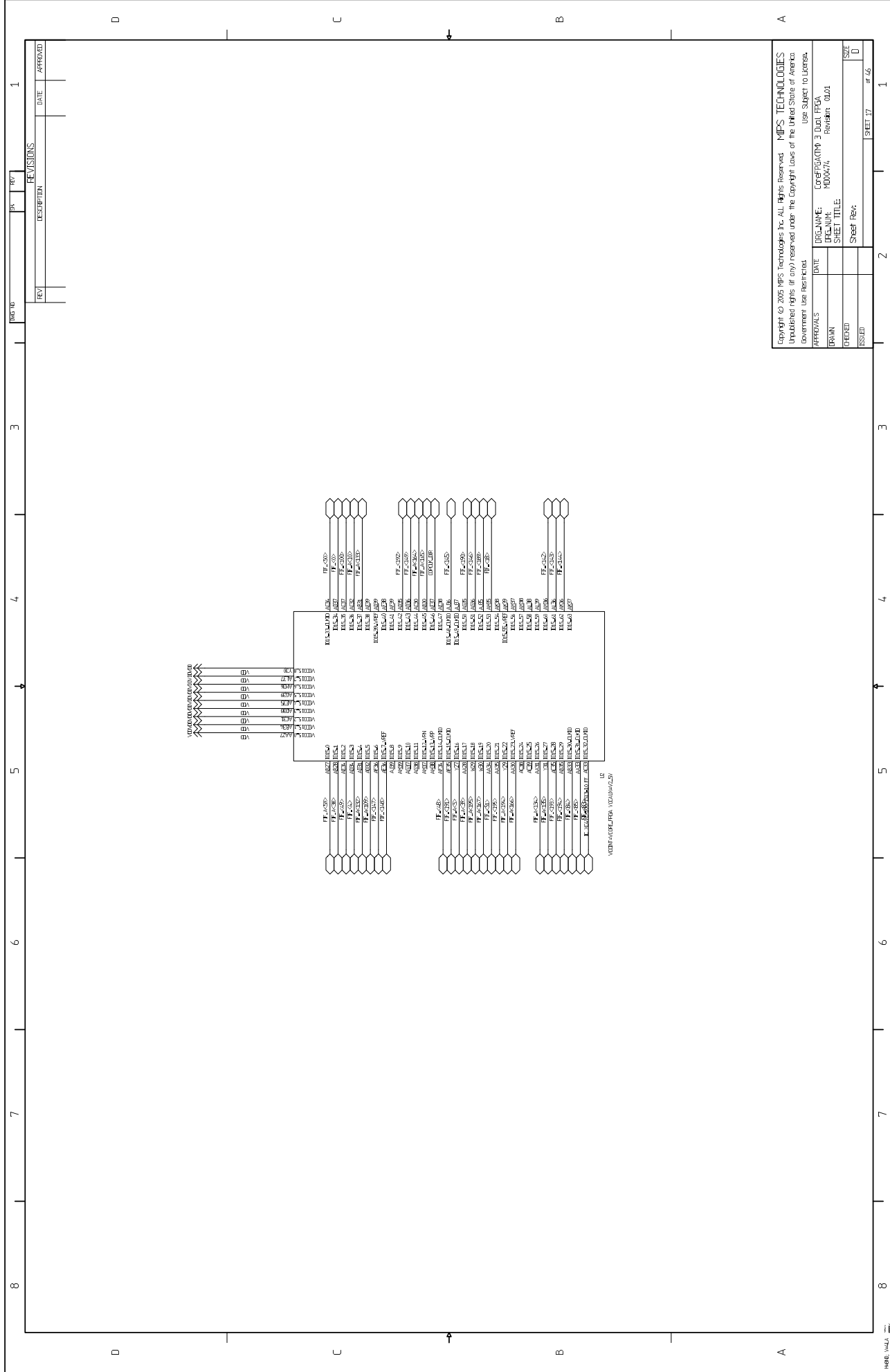
REV	DESCRIPTION	DATE	APPROVED

Copyright © 2005 MIPS Technologies, Inc. All Rights Reserved. MIPS TECHNOLOGIES Unpublished MIPS (if any) reserved under the Copyright Laws of the United States of America. Government Use Restricted.	
DATE	COEFFICIENT 3 Dual FPGA
DRAWN	1000474
CHECKED	1000474
ISSUED	1000474
Sheet No.	15 of 16
Sheet Title	COEFFICIENT 3 Dual FPGA
Sheet Rev.	0.01
SIZE	D



REV	DESCRIPTION	DATE	APPROVED

Copyright © 2005 MIPS Technologies, Inc. All Rights Reserved. MIPS TECHNOLOGIES Unpublished MIPS (if any) reserved under the Copyright Laws of the United States of America. Government Use Restricted. Use Subject to License.	
DATE	06/14/05
DWG NAME	COREFPGA3_3 Dual FPGA
DWG NO	1000474
SHEET TITLE	Reboardr 01A1
DRAWN	
CHECKED	
ISSUED	
Sheet No.	1
Sheet Tot.	1

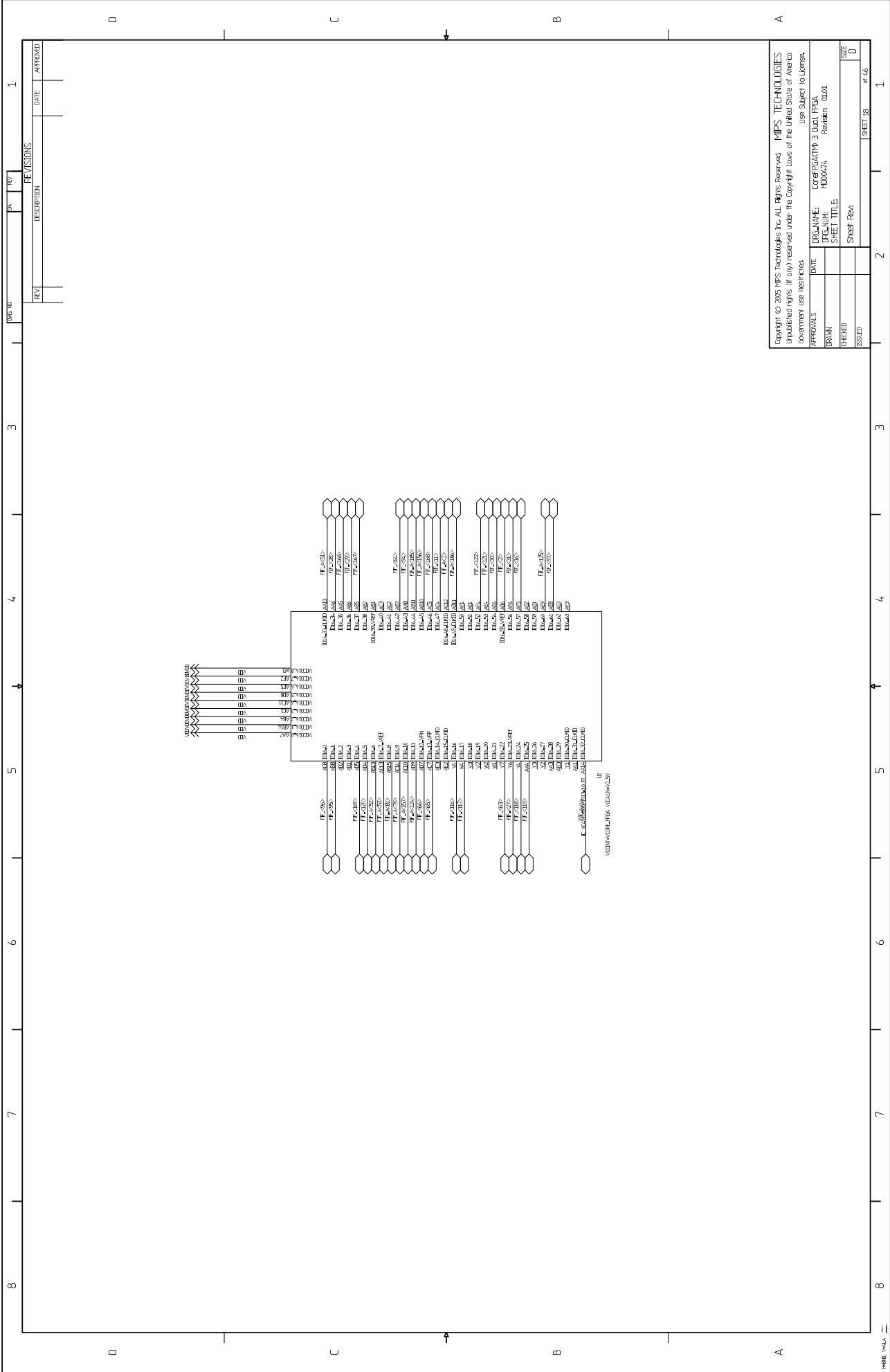


REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

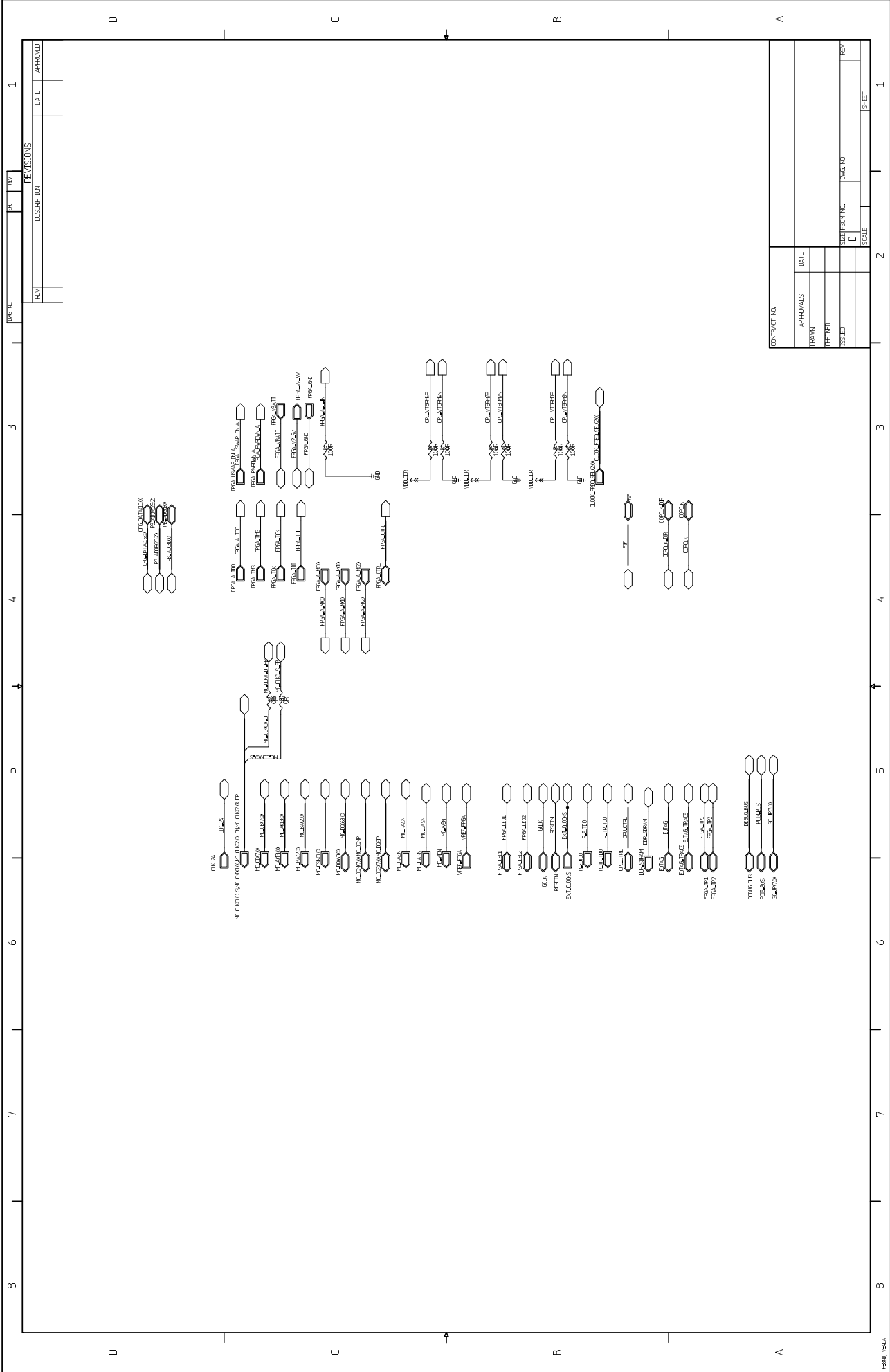
DATE	DESIGNER	DATE	DESIGNER

DATE	DESIGNER	DATE	DESIGNER



REV	DESCRIPTION	DATE	APPROVED

Copyright © 2005 MIPS Technologies, Inc. All Rights Reserved. MIPS TECHNOLOGIES Unpublished MIPS (if any) reserved under the Copyright Laws of the United States of America Government Use Restricted	
DATE	COEFFICIENT 3 Dual FPGA
DWG NAME	1000474
SHEET TITLE	Rebuild: 01.01
CHECKED	Sheet Rev:
ISSUED	SHEET 18 of 46



REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

IC1	IC2	IC3	IC4	IC5	IC6	IC7	IC8	IC9	IC10
-----	-----	-----	-----	-----	-----	-----	-----	-----	------

R1	R2	R3	R4	R5	R6	R7	R8	R9	R10
----	----	----	----	----	----	----	----	----	-----

C1	C2	C3	C4	C5	C6	C7	C8	C9	C10
----	----	----	----	----	----	----	----	----	-----

U1	U2	U3	U4	U5	U6	U7	U8	U9	U10
----	----	----	----	----	----	----	----	----	-----

Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10
----	----	----	----	----	----	----	----	----	-----

W1	W2	W3	W4	W5	W6	W7	W8	W9	W10
----	----	----	----	----	----	----	----	----	-----

CON1	CON2	CON3	CON4	CON5	CON6	CON7	CON8	CON9	CON10
------	------	------	------	------	------	------	------	------	-------

RES1	RES2	RES3	RES4	RES5	RES6	RES7	RES8	RES9	RES10
------	------	------	------	------	------	------	------	------	-------

DIODE1	DIODE2	DIODE3	DIODE4	DIODE5	DIODE6	DIODE7	DIODE8	DIODE9	DIODE10
--------	--------	--------	--------	--------	--------	--------	--------	--------	---------

IND1	IND2	IND3	IND4	IND5	IND6	IND7	IND8	IND9	IND10
------	------	------	------	------	------	------	------	------	-------

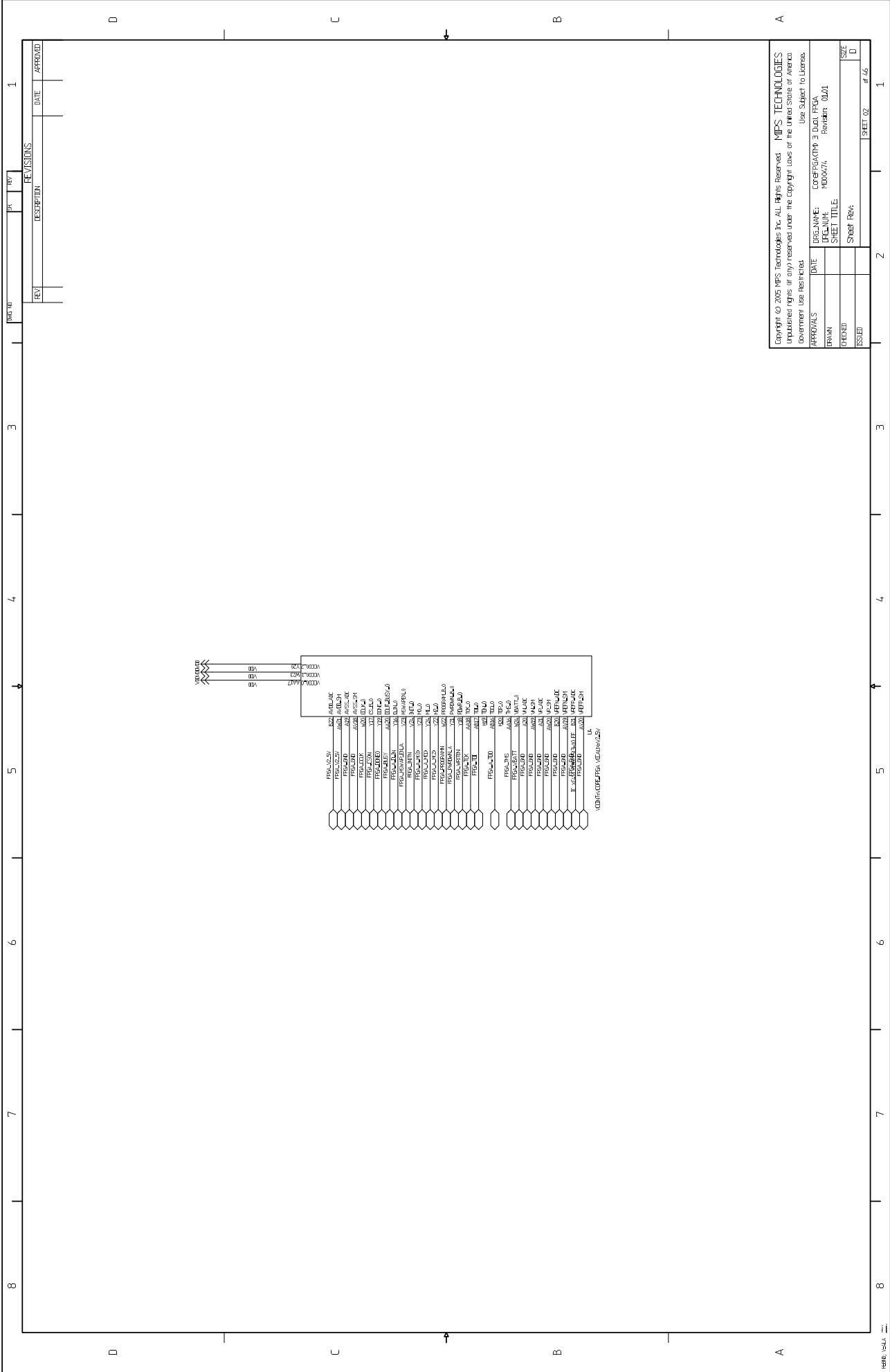
VAR1	VAR2	VAR3	VAR4	VAR5	VAR6	VAR7	VAR8	VAR9	VAR10
------	------	------	------	------	------	------	------	------	-------

SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW9	SW10
-----	-----	-----	-----	-----	-----	-----	-----	-----	------

CONN1	CONN2	CONN3	CONN4	CONN5	CONN6	CONN7	CONN8	CONN9	CONN10
-------	-------	-------	-------	-------	-------	-------	-------	-------	--------

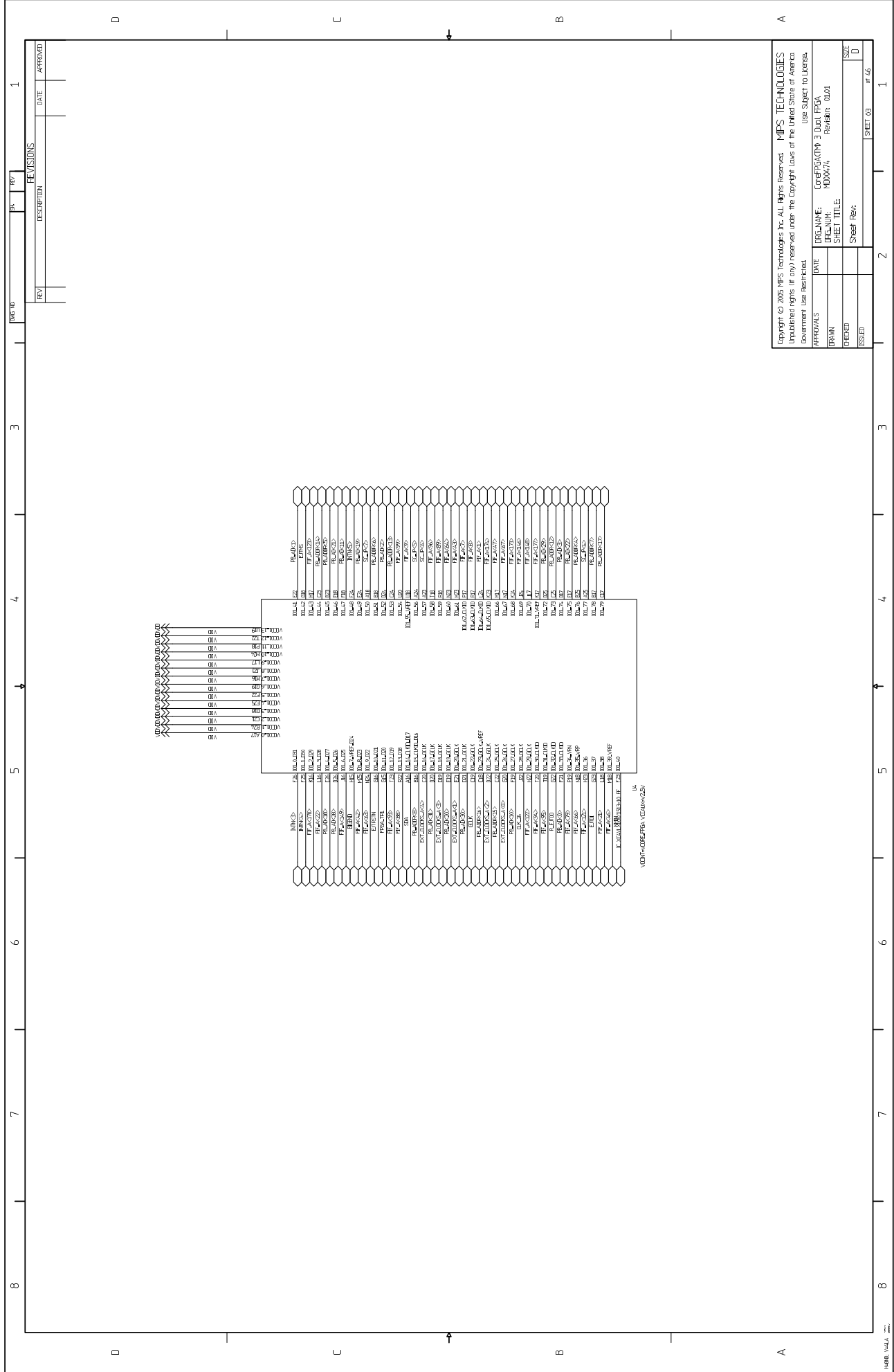
IC1	IC2	IC3	IC4	IC5	IC6	IC7	IC8	IC9	IC10
-----	-----	-----	-----	-----	-----	-----	-----	-----	------

IC1	IC2	IC3	IC4	IC5	IC6	IC7	IC8	IC9	IC10
-----	-----	-----	-----	-----	-----	-----	-----	-----	------



REV	DESCRIPTION	DATE	APPROVED

Copyright © 2005 MIPS Technologies, Inc. All Rights Reserved. MIPS TECHNOLOGIES Unpublished rights (if any) reserved under the Copyright Laws of the United States of America. Government Use Restricted. Use Subject to License.	
DATE	DESIGN NAME
	COREPGA03 (DUAL FPGA)
	DESIGN NO.
	10000074
	SHEET TITLE
	Revision: 00.01
DRAWN	CHECKED
ISSUED	Sheet Rev:
	SHEET 02 of 06



REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

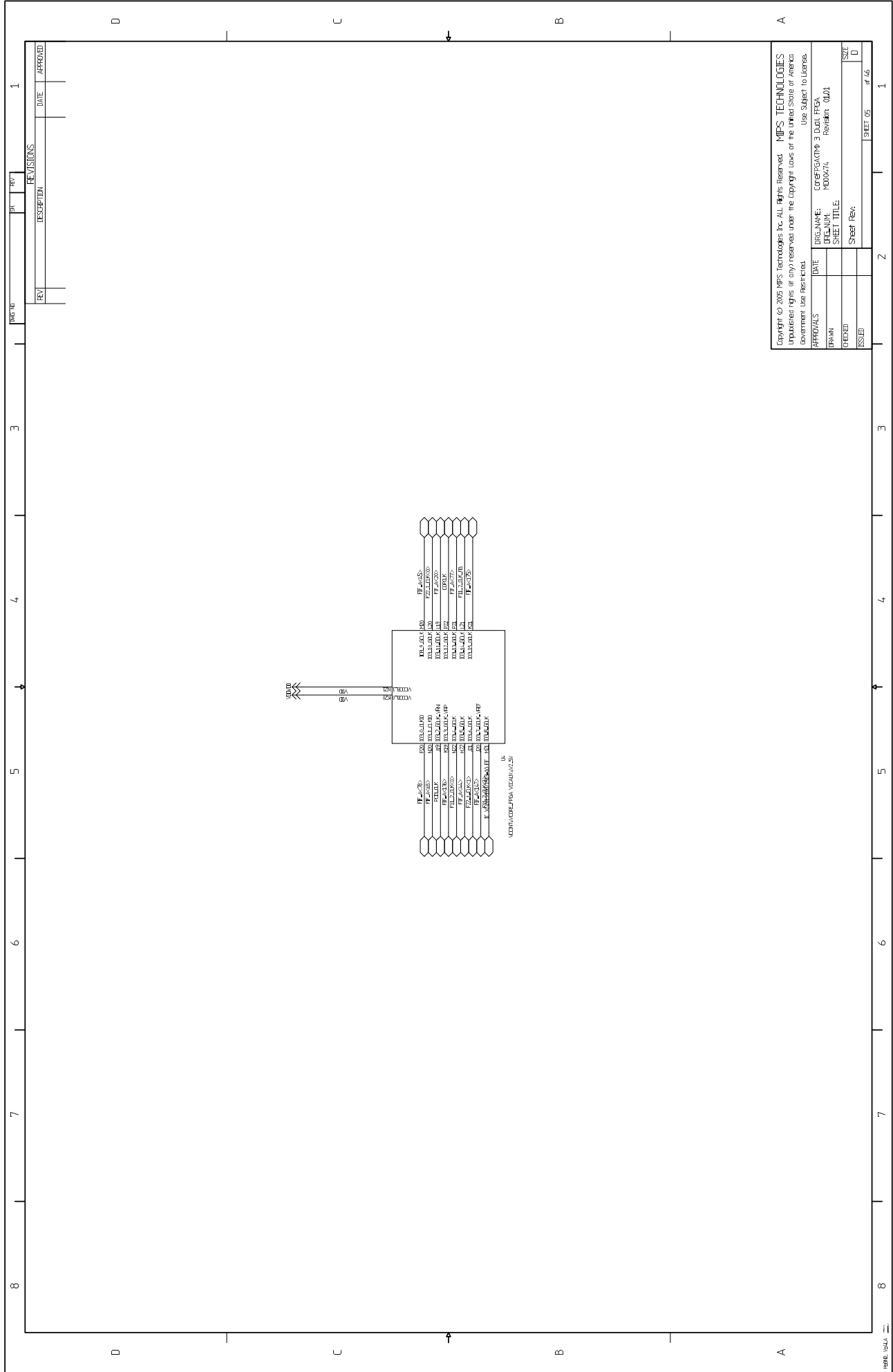
Copyright © 2005 MIPS Technologies, Inc. All Rights Reserved. MIPS TECHNOLOGIES
 Unpublished Rights (if any) reserved under the Copyright Laws of the United States of America
 Government Use Restricted

APPROVALS

DATE	DESIGNER	DATE	DESIGNER

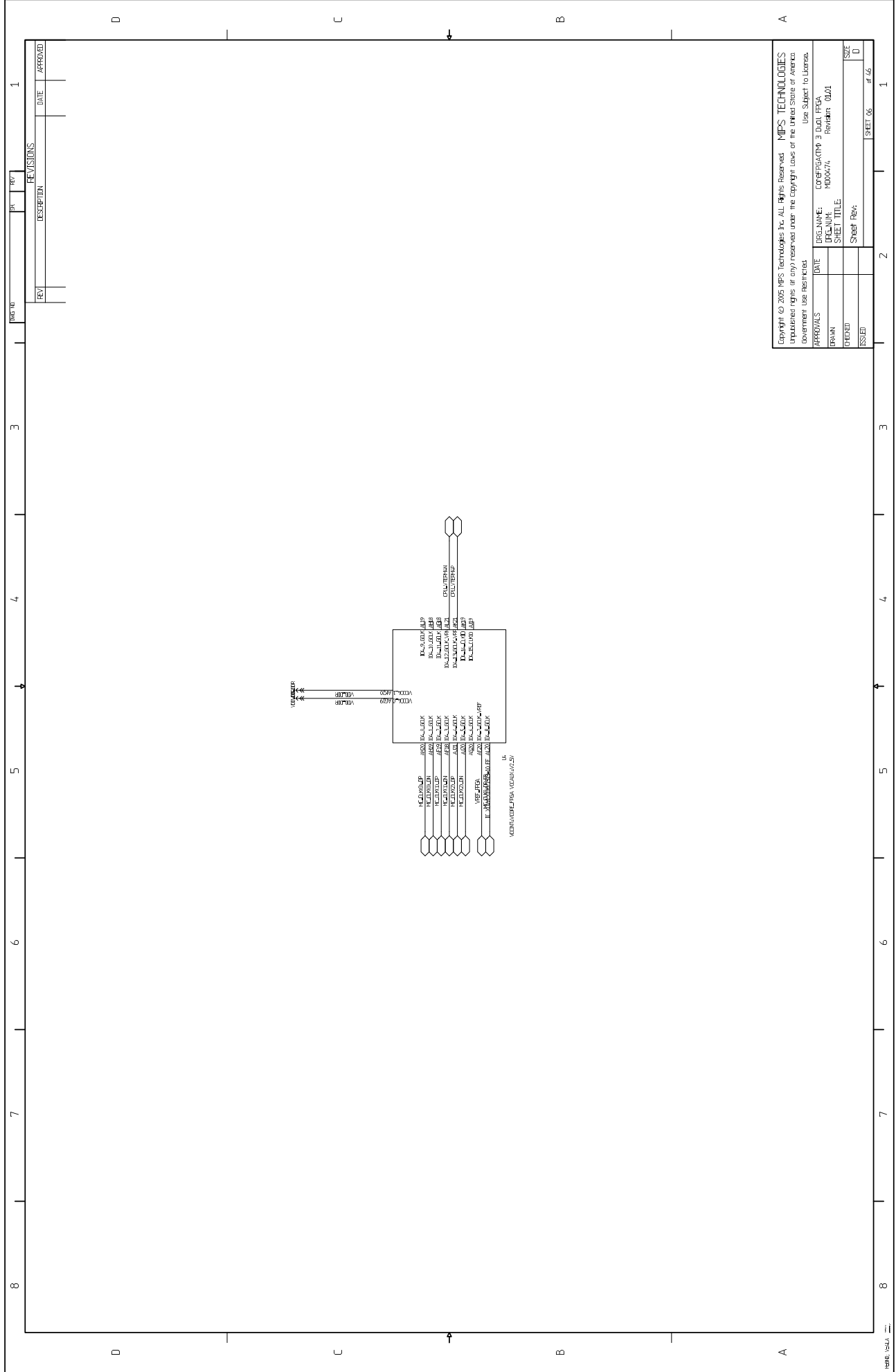
DRAWN: COEFFICIENT 3 DUAL FPGA
 CHECKED: H000474
 SHEET TITLE: Revision: 0.0.1

ISSUED: Sheet Rev: 0.0.1



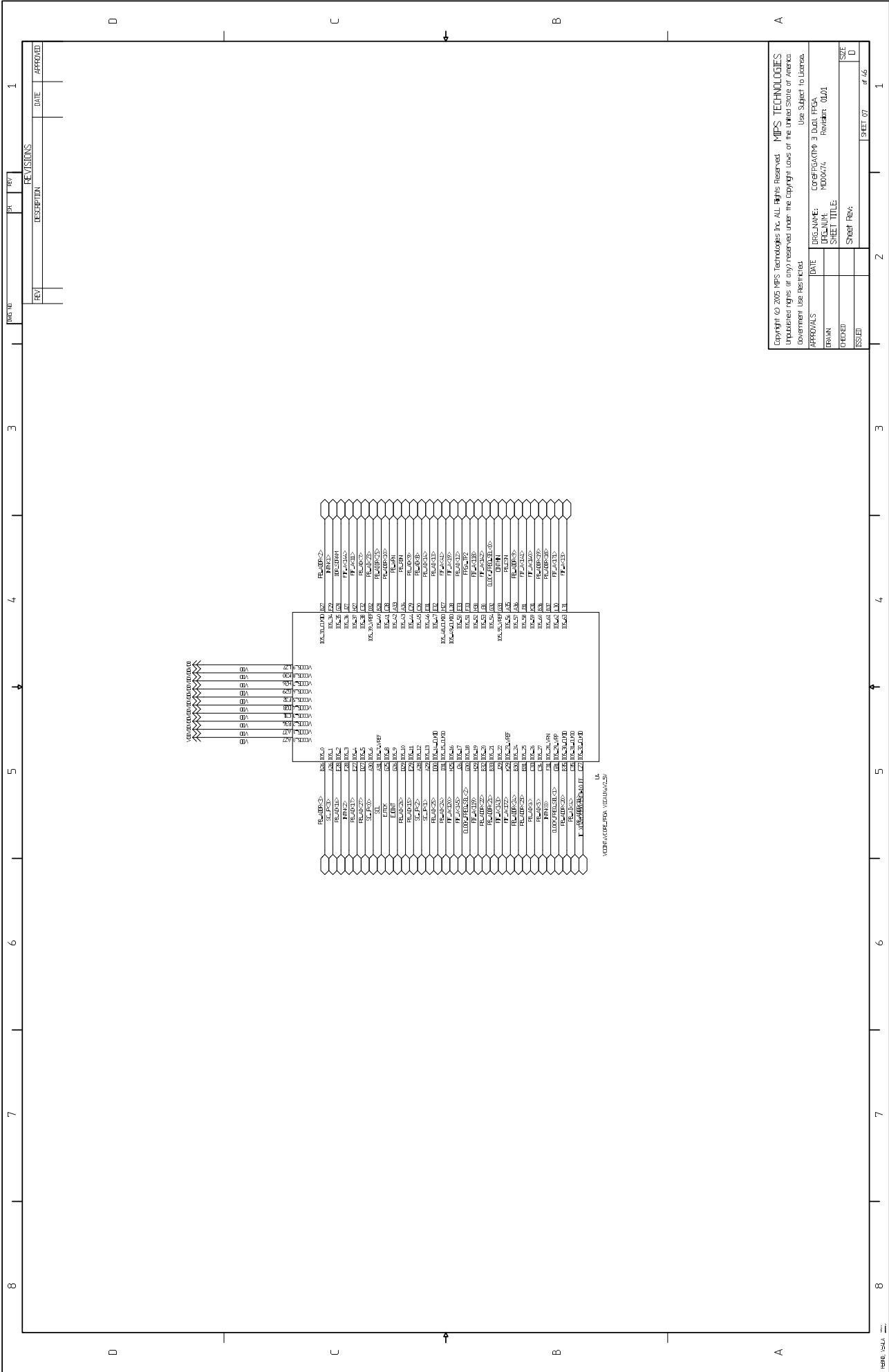
REV	DESCRIPTION	DATE	APPROVED

Copyright © 2005 MIPS Technologies, Inc. All Rights Reserved. MIPS TECHNOLOGIES Unpublished rights (if any) reserved under the Copyright Laws of the United States of America. Government Use Restricted. Use Subject to License.			
DATE	DESIGNER	DATE	APPROVED
CHECKED	ISSUED	SHEET 05	of 06

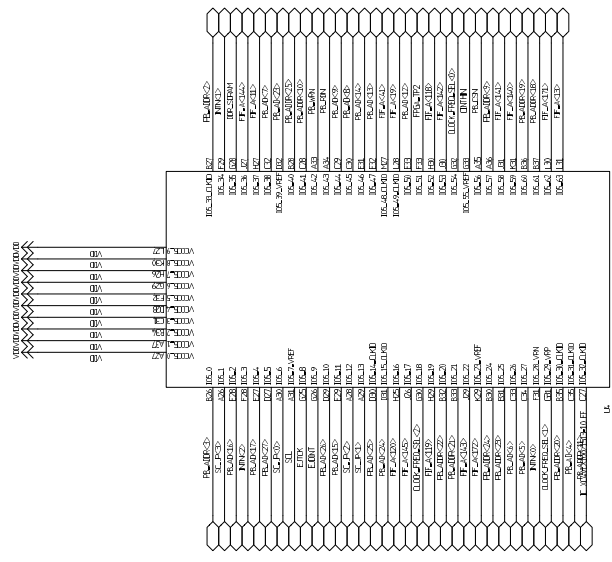


REV	DESCRIPTION	DATE	APPROVED

Copyright © 2005 MIPS Technologies, Inc. All Rights Reserved. MIPS TECHNOLOGIES	
Unpublished rights (if any) reserved under the Copyright Laws of the United States of America.	
Government Use Restricted Use Subject to License.	
DATE	DESIGN NAME: CONFIDENTIAL 3 DUAL UPGA
DRAWN	DRAWN BY: H000074
CHECKED	SHEET TITLE: Revision: 0001
ISSUED	Sheet Rev:
	SIZE: D
	SHEET 06 of 06

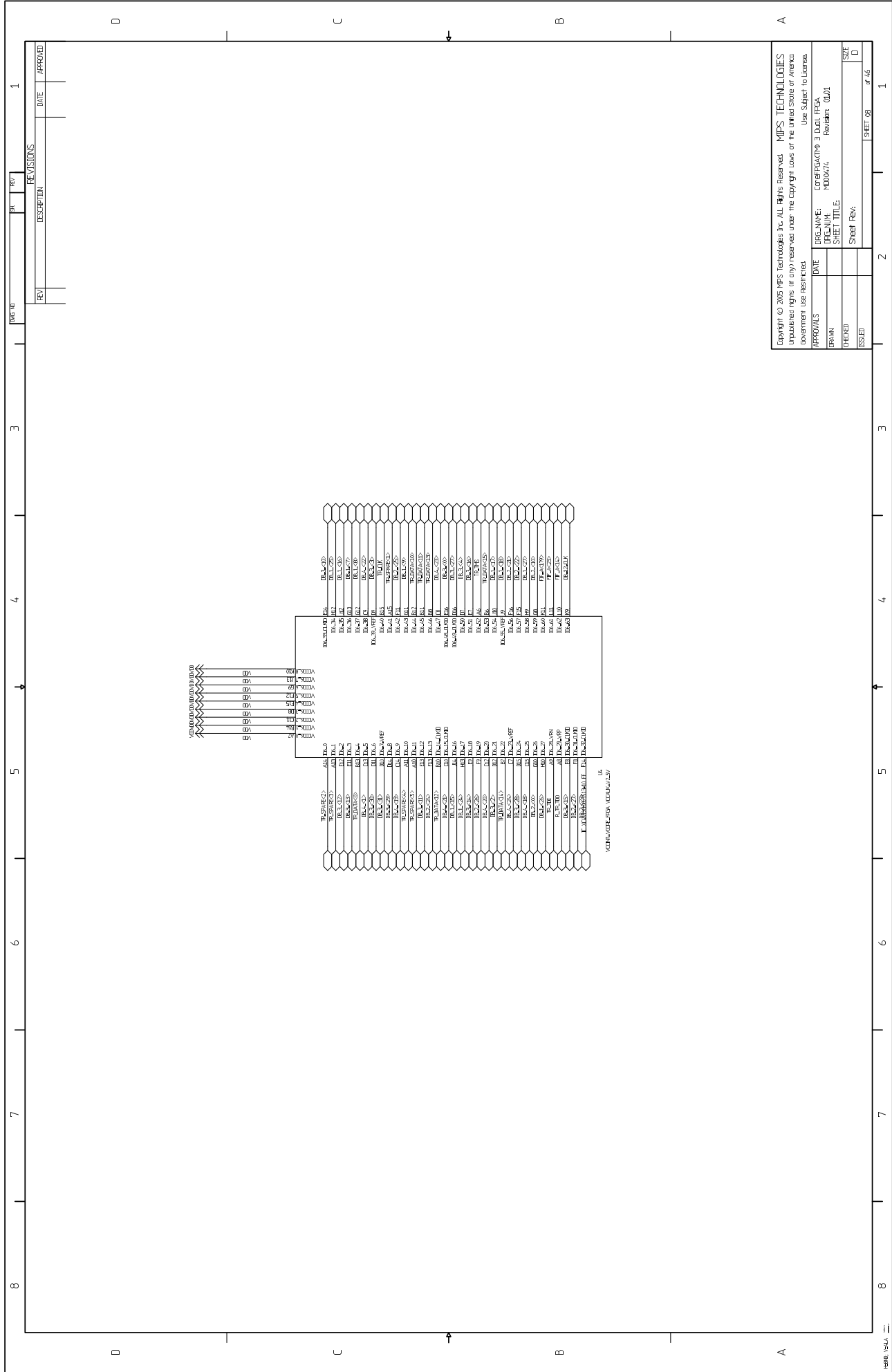


REV	DESCRIPTION	DATE	APPROVED



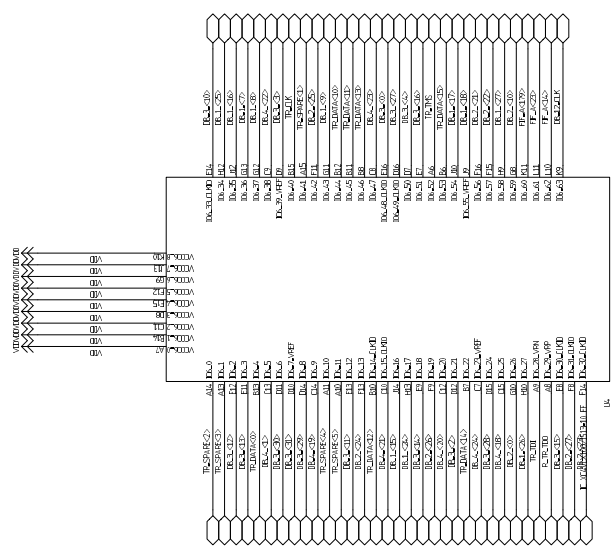
APPROVALS		DATE	DESIGN NAME	DATE	DESIGN NAME
DRAWN	CHECKED	ISSUED	PROJECT NO.	REV	DESCRIPTION

Copyright © 2005 MIPS Technologies, Inc. All Rights Reserved. MIPS TECHNOLOGIES
 Unpublished rights: (if any) reserved under the Copyright Laws of the United States of America
 Government Use Restricted
 Use Subject to License



REV	DESCRIPTION	DATE	APPROVED

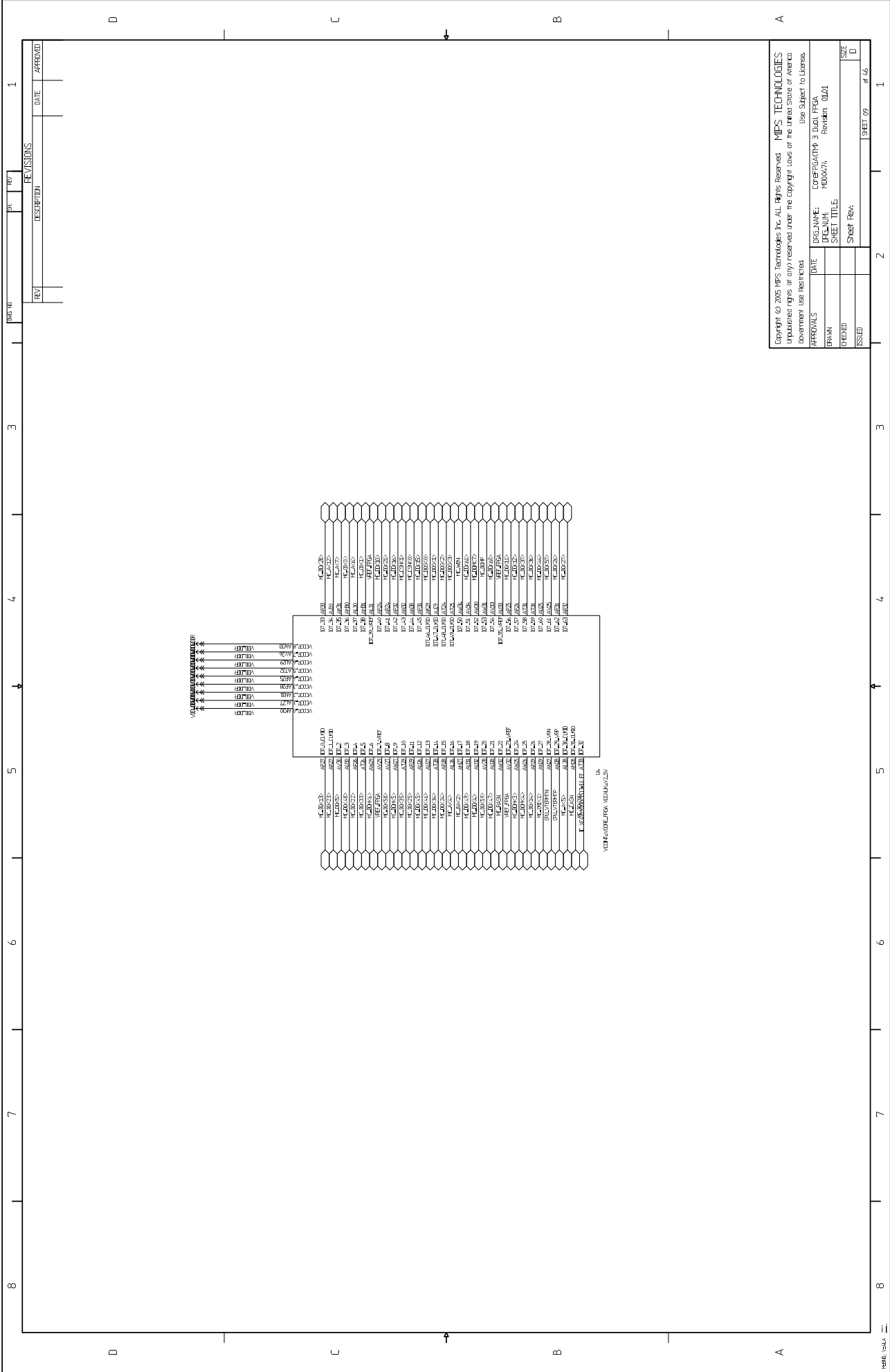
REV	REV



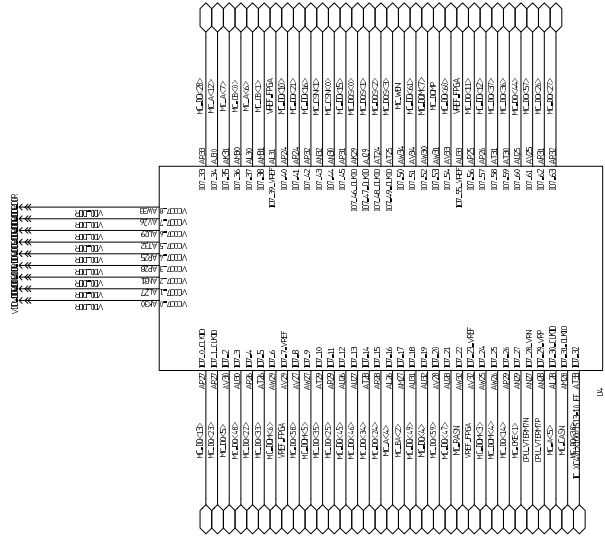
Copyright © 2005 MIPS Technologies, Inc. All Rights Reserved. MIPS TECHNOLOGIES
 Unpublished rights (if any) reserved under the Copyright Laws of the United States of America.
 Government Use Restricted.

APPROVALS	DATE	DESIGN NAME	CORRELATING 3 DUAL LEGAL
DRAWN		DRAWN BY	10000474
CHECKED		SHEET TITLE	Revisort: 0001
ISSUED		Sheet Rev:	

SIZE
D



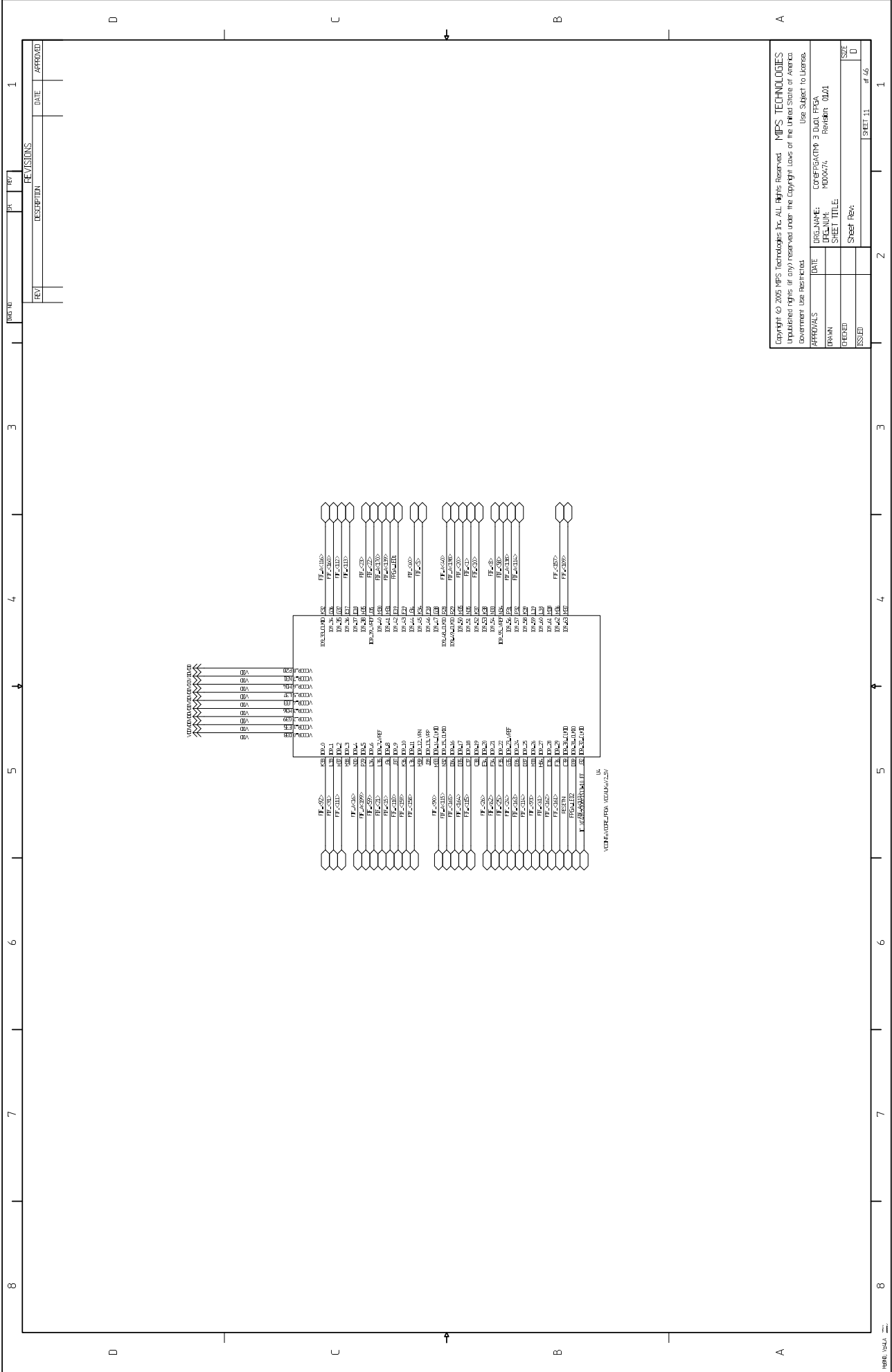
REV	DESCRIPTION	DATE	APPROVED



Copyright © 2005 MIPS Technologies, Inc. All Rights Reserved. MIPS TECHNOLOGIES
 Unpublished rights (if any) reserved under the Copyright Laws of the United States of America.
 Government Use Restricted. Use Subject to License.

APPROVALS	DATE	DESIGN NAME	CORRELATING 3 DUAL ITEMS
DRAWN		DRAWN BY	10000474
CHECKED		SHEET TITLE	Reconnect_0001
ISSUED		Sheet Rev:	

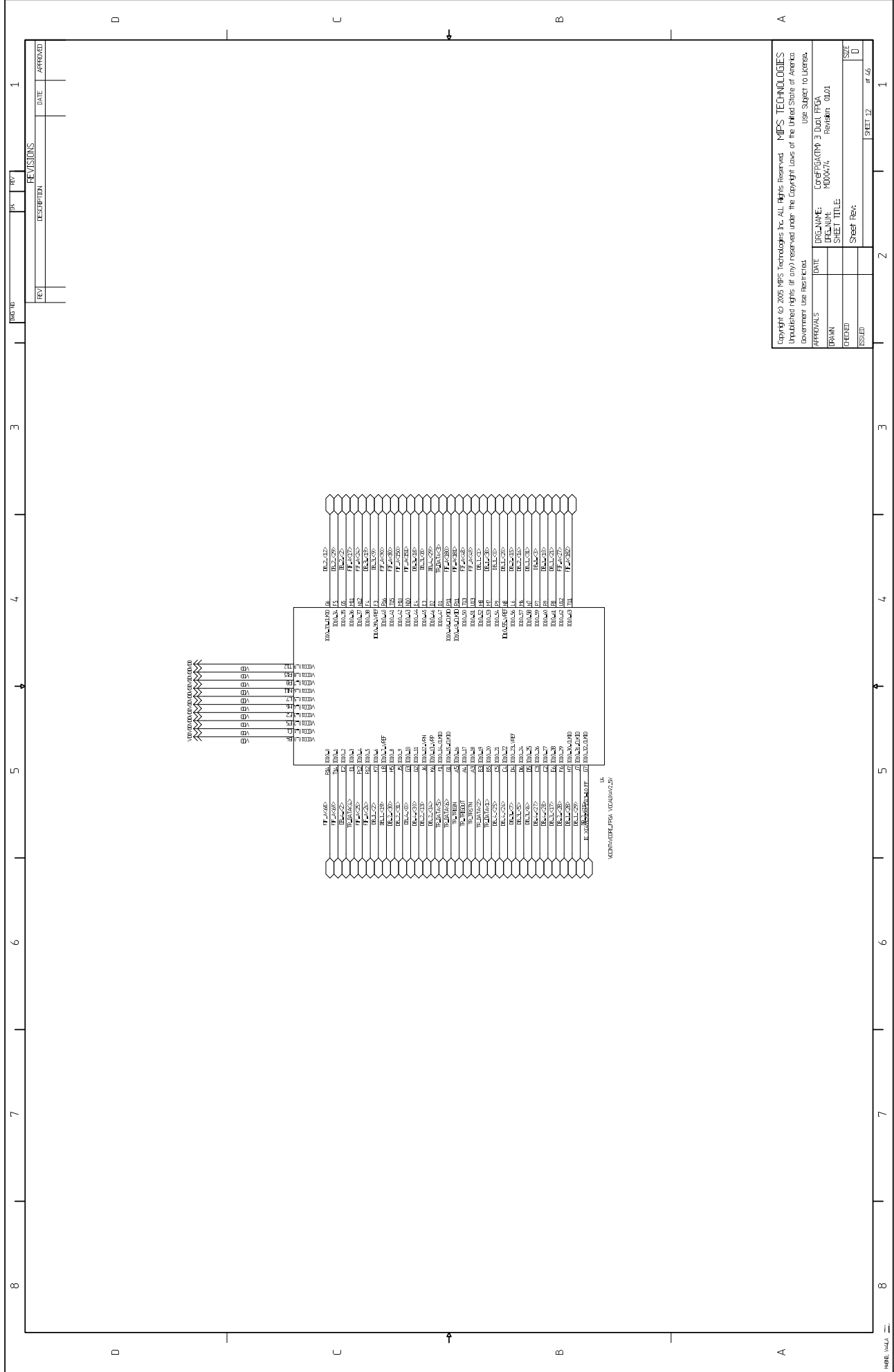
SIZE: D
 SHEET 09 of 46



REV	DESCRIPTION	DATE	APPROVED

APPROVALS		DATE		DESIGN NAME		PROJECT NAME		SHEET TITLE	
DRAWN	CHECKED	ISSUED							

Copyright © 2005 MIPS Technologies, Inc. All Rights Reserved. MIPS TECHNOLOGIES
 Unpublished rights (if any) reserved under the Copyright Laws of the United States of America
 Government Use Restricted
 Use Subject to License



REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

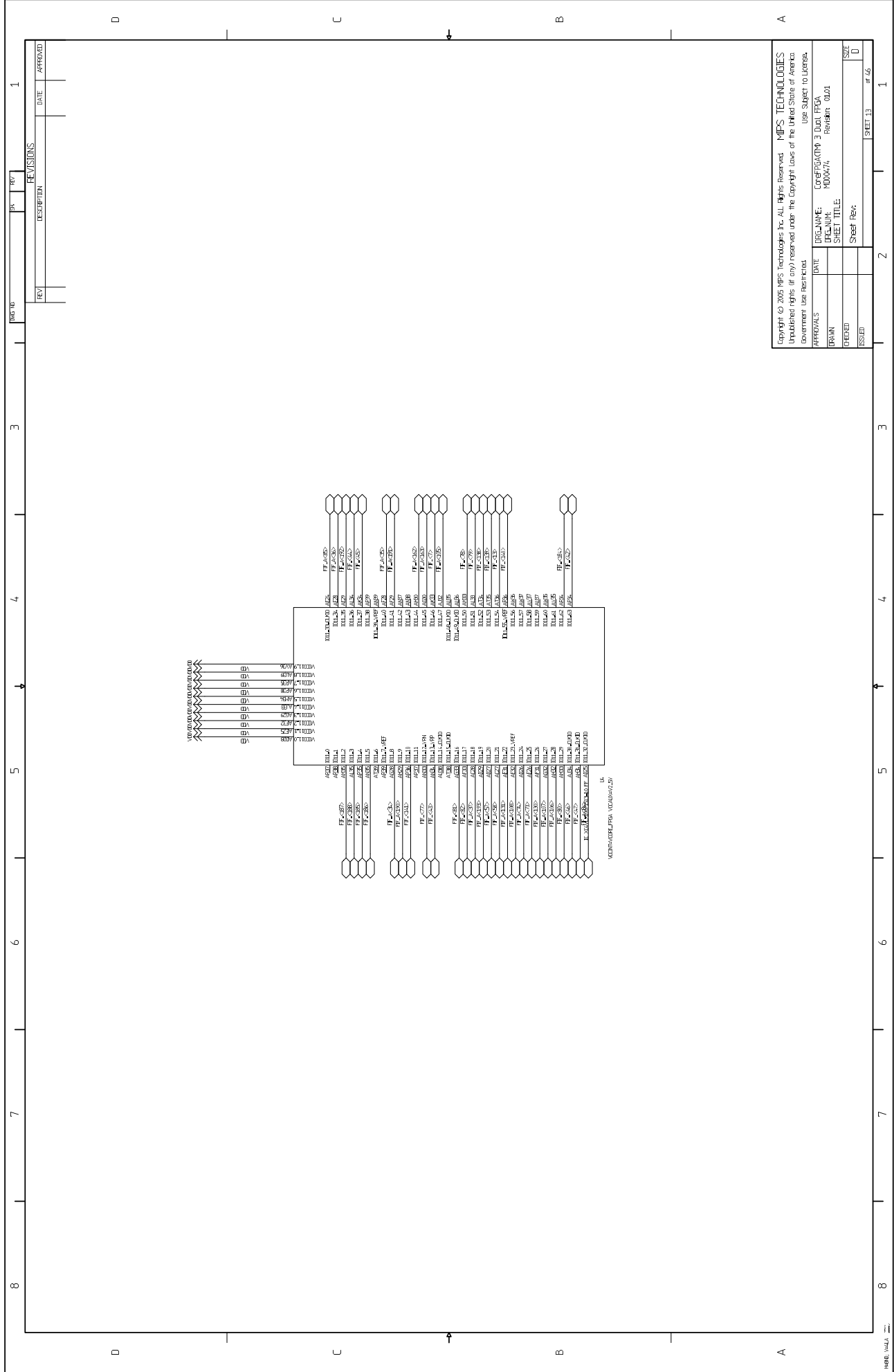
REV	DESCRIPTION	DATE	APPROVED

DATE		DATE	
DRAWN		CHECKED	
ISSUED		SHEET 12 OF 46	

Copyright © 2005 MIPS Technology, Inc. All Rights Reserved. MIPS TECHNOLOGIES
 Unpublished MIPS (if any) reserved under the Copyright Laws of the United States of America.
 Government Use Restricted. Use Subject to License.

DESIGN NAME: COFFEINATING 3 DUAL FPGA
 DIAL NAME: H000474
 SHEET TITLE: Boardrht_0101

Sheet Rev: 0
 SIZE: D



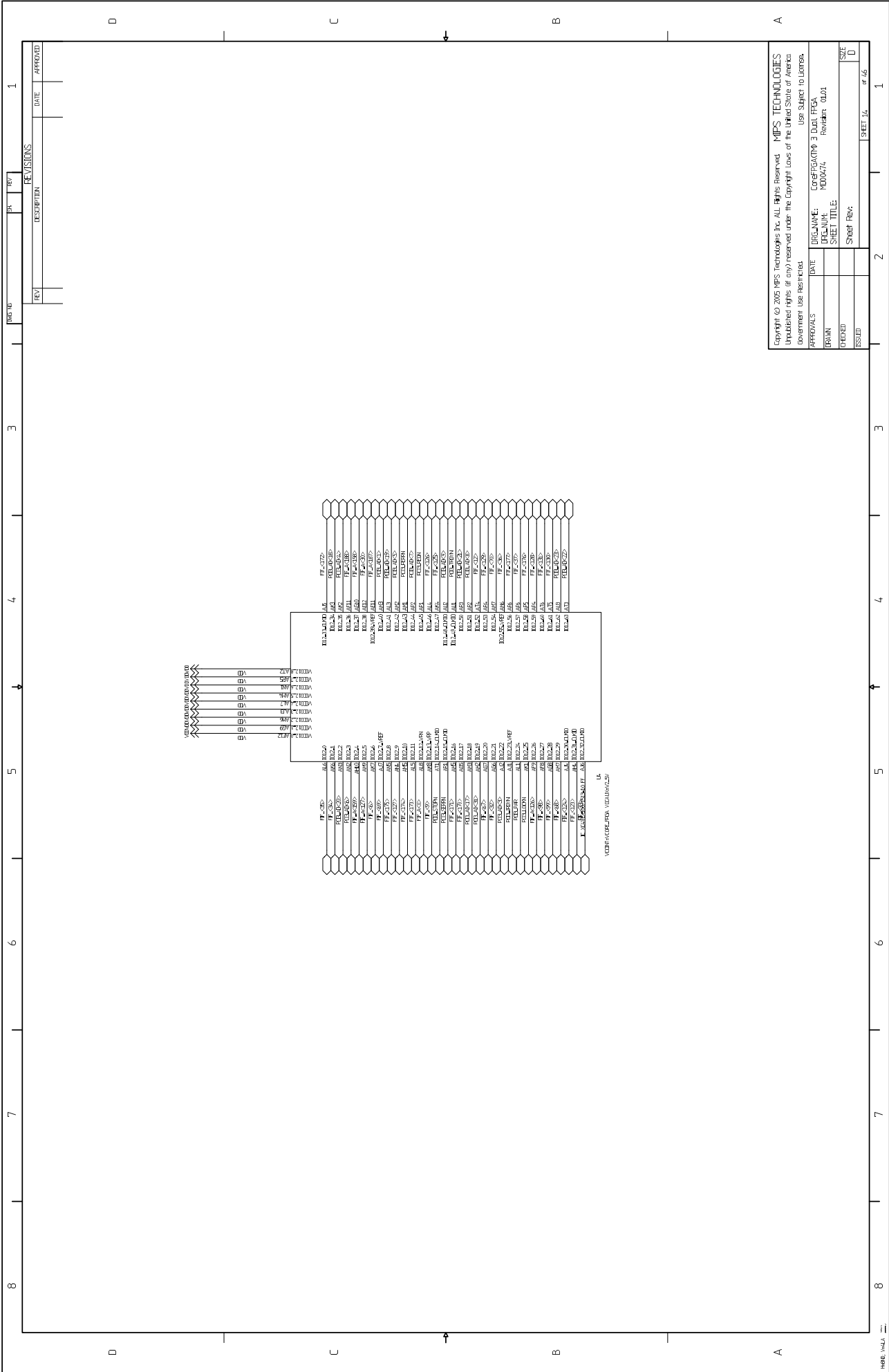
REV	DESCRIPTION	DATE	APPROVED

APPROVALS		DATE	DESIGN NAME	PROJECT NO.	REV
DRAWN	CHECKED	ISSUED	SHEET TITLE		

Copyright © 2005 MIPS Technologies, Inc. All Rights Reserved. MIPS TECHNOLOGIES
 Unpublished MIPS (if any) reserved under the Copyright Laws of the United States of America
 Government Use Restricted Use Subject to License

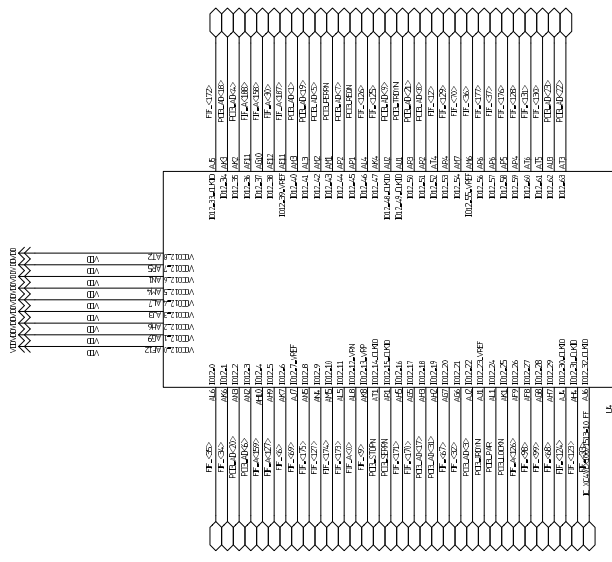
DESIGN NAME: COFFEINATING 3 Dual FPGA
 PROJECT NO: 1000474
 SHEET TITLE: Revision: 01.01

Sheet Rev: 13 of 46
 SHEET 13 of 46



REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED



DATE	DESIGNER	DATE	DESIGNER

DATE	DESIGNER	DATE	DESIGNER

DATE	DESIGNER	DATE	DESIGNER

DATE	DESIGNER	DATE	DESIGNER

DATE	DESIGNER	DATE	DESIGNER

DATE	DESIGNER	DATE	DESIGNER

DATE	DESIGNER	DATE	DESIGNER

DATE	DESIGNER	DATE	DESIGNER

DATE	DESIGNER	DATE	DESIGNER

DATE	DESIGNER	DATE	DESIGNER

DATE	DESIGNER	DATE	DESIGNER

DATE	DESIGNER	DATE	DESIGNER

DATE	DESIGNER	DATE	DESIGNER

DATE	DESIGNER	DATE	DESIGNER

DATE	DESIGNER	DATE	DESIGNER

DATE	DESIGNER	DATE	DESIGNER

DATE	DESIGNER	DATE	DESIGNER

DATE	DESIGNER	DATE	DESIGNER

DATE	DESIGNER	DATE	DESIGNER

DATE	DESIGNER	DATE	DESIGNER

DATE	DESIGNER	DATE	DESIGNER

DATE	DESIGNER	DATE	DESIGNER

DATE	DESIGNER	DATE	DESIGNER

DATE	DESIGNER	DATE	DESIGNER

DATE	DESIGNER	DATE	DESIGNER

DATE	DESIGNER	DATE	DESIGNER

DATE	DESIGNER	DATE	DESIGNER

DATE	DESIGNER	DATE	DESIGNER

DATE	DESIGNER	DATE	DESIGNER

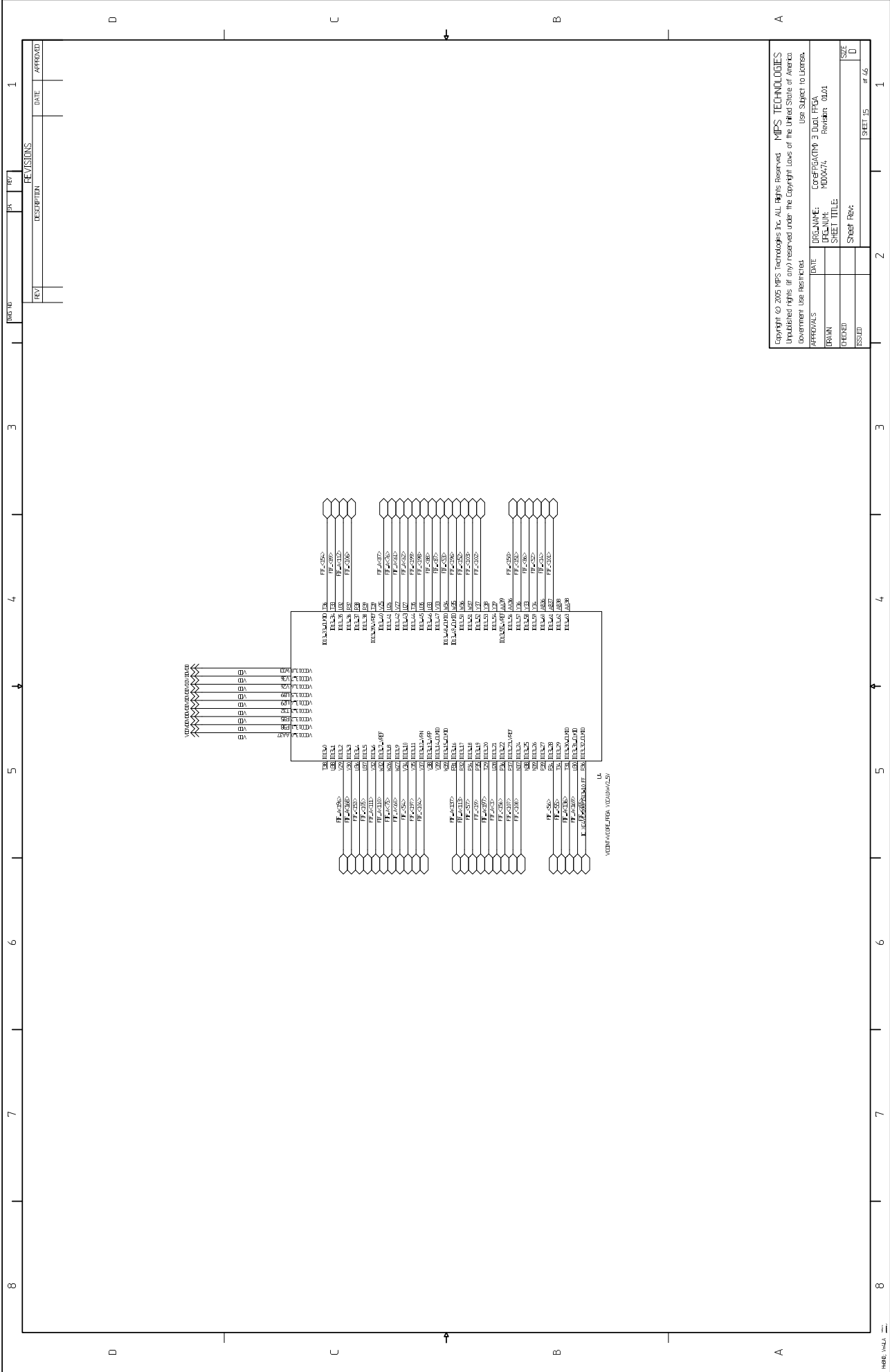
DATE	DESIGNER	DATE	DESIGNER

DATE	DESIGNER	DATE	DESIGNER

DATE	DESIGNER	DATE	DESIGNER

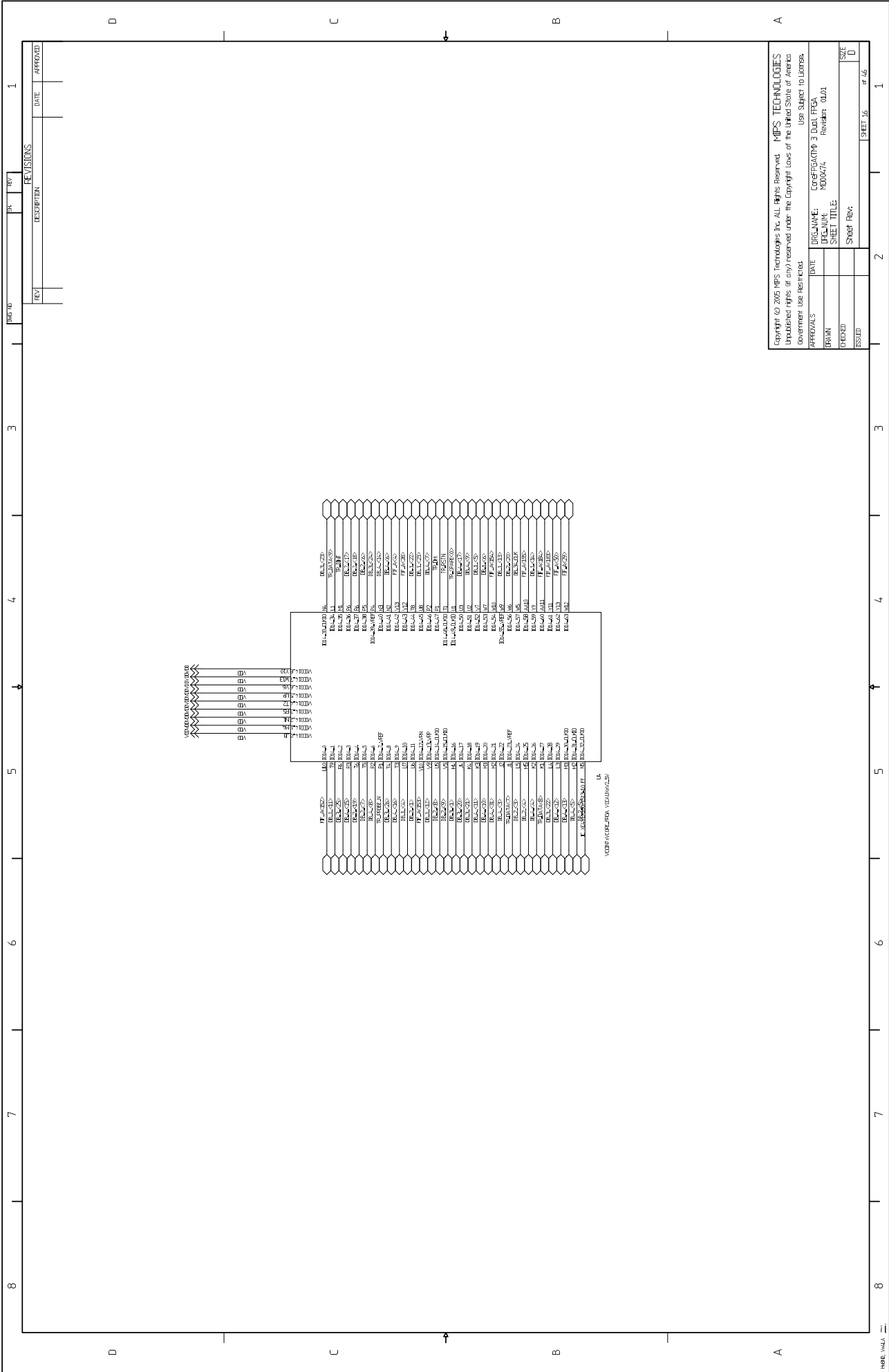
DATE	DESIGNER	DATE	DESIGNER

DATE	DESIGNER	DATE	DESIGNER



REV	DESCRIPTION	DATE	APPROVED

Copyright © 2005 MIPS Technologies, Inc. All Rights Reserved. MIPS TECHNOLOGIES Unpublished MIPS (if any) reserved under the Copyright Laws of the United States of America. Government Use Restricted.	
DATE	10/04/05
DWG. NAME	CORE_FPGA3_DUAL_FPGA
DRAWN	10/04/05
CHECKED	10/04/05
ISSUED	10/04/05
SHEET TITLE	10/04/05
Sheet No.	15 of 16
SIZE	D



REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

REV	DESCRIPTION	DATE	APPROVED

Copyright © 2005 MIPS Technology, Inc. All Rights Reserved. MIPS TECHNOLOGIES Unpublished MIPS (if any) reserved under the Copyright Laws of the United States of America. Government Use Restricted	
DATE	COEFFICIENT 3 Dual FPGA
DRAWN	1000474
CHECKED	1000474
ISSUED	Sheet Rev: 0
	Sheet 16 of 16

